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# Low Frequency Noise Modeling in Single- and Double-Gate MOSFETs

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# Low Frequency Noise Modeling in Single- and Double-Gate MOSFETs

by

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# ABSTRACT

The Flicker or $1/f$ noise dominates the noise spectrum at low frequency. A serious concern for MOSFETs for circuit application is much higher flicker ($1/f$) noise because of the heterogeneous interface between silicon (Si) and silicon dioxide ($SiO_2$). Very high intrinsic flicker noise of CMOS transistors becomes a drawback for low-Intermediate Frequency (IF) or direct-conversion architectures. In spite of extensive research and efforts to understand the low-frequency noise origin in semiconductor devices, there exists no unique theory to explain the low-frequency noise generation mechanism. Flicker noise in MOSFETs is usually perceived to be caused by carrier density fluctuations, which is result of interaction of free carriers with oxide traps via interface states. The most widely accepted theories to explain the flicker noise generation mechanism in MOSFETs are the number fluctuation model proposed by McWhorter based on the tunneling transitions between traps in the oxide and channel carriers, and the mobility fluctuation model, which is described by Hooge's empirical relation. Correlated low frequency noise models, which incorporate both the number fluctuation and correlated surface mobility fluctuation, have also been studied. This work presents a physics-based, analytical model for low-frequency or $1/f$ noise in single- and double-gate MOSFETs. The model is an extension of a correlated low frequency noise model. The developed model takes into account the effects of quantization in the silicon channel, short channel characteristics of the device, and effective trap levels contributing to low-frequency noise generation mechanism. The inclusion of quantum effects is based on a self-consistent solution of Poisson and Schrödinger equations in the silicon inversion

layer. For low-frequency noise calculation, both the number induced and correlated mobility-induced perturbations caused by the channel carriers' interactions with the oxide states are considered. The physical parameter, effective oxide trap levels at the semiconductor-insulator interface, is modeled using the Hooge parameter and is correlated with inversion charge of the device. The model has been used to predict the low-frequency noise characteristics of a single-gate (bulk) device, a single-gate (SOI) device and a double-gate (SOI) device.

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1. S. Rai, and S. Islam, "Low frequency noise modeling in single- and double-gate MOSFETs," *Journal of Applied Physics,* To be submitted .

## Conference

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*Chapter 1*

# Introduction



## 1.1 Introduction

The definition of noise is "A disturbance that obscures or reduces the clarity of a signal". The source of this noise can be classified into two categories. One is artificial noise created by numerous noise sources from the environment. The other source of noise is fundamental noise created by the circuits or devices. The intrinsic noise in a semiconductor device is generated by several different mechanisms. In Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs), there are two major sources of noise: flicker ($1/f$) noise and thermal noise. The name "flicker noise" refers to noise phenomena with a spectrum of the form $AI^{\beta}/f^{\alpha}$, where $A$ is a constant, $I$ is the current, $f$ is the frequency, and the exponents $\beta$ and $\alpha$ are empirical constants. Flicker noise dominates the noise spectrum at low frequency. Flicker noise was first observed in vacuum tubes seventy-nine years ago [1]. It gets its name from the anomalous "flicker" that was seen in the plate current. Flicker noise is also commonly called $1/f$ noise, because the noise spectrum varies as $1/f^{\alpha}$, where the exponent $\alpha$ is very close to unity ($\alpha = 1 \pm 0.2$). Fluctuations with a $1/f$ power law have been observed in practically all

electronic materials and devices, including homogenous semiconductors, junction devices, metal films, liquid metals, electrolytic solutions, *etc.* In addition it has been observed in mechanical, biological, geological, and even musical systems.

MOSFETs have emerged as a good substitute for bipolar junction transistors (BJTs) in analog and RF circuit applications. However, a serious concern for MOSFETs in analog circuits is much higher flicker ($1/f$) noise because of the heterogeneous interface between silicon (Si) and silicon dioxide ($SiO_2$). Low-frequency noise, also known as $1/f$ noise, is observed in almost every electron device and has been the center of attention for the last few decades [2]. Recent advances in process technology allow the realization of ultra low-power consumption RF CMOS receivers operating in the multi-GHz frequency range with a supply voltage as low as 1 V [3]. The flicker or $1/f$ noise dominates the noise spectrum at low frequency and very high intrinsic flicker noise of CMOS transistors becomes a drawback for low-Intermediate Frequency (IF) or direct-conversion architectures. The flicker noise raises the noise floor accompanying the signal, which has been translated to zero IF, in the baseband circuits. It can be a detrimental factor in the performance of high-frequency nonlinear circuits such as mixers and oscillators. In the down-conversion mixer, it significantly degrades the noise figure at low output IF. In Voltage Controlled Oscillators (VCO), the low frequency noise raises the phase noise at the 25 kHz offset where the adjacent channel lies. For the scaled-down transistors required by RF circuits, the $1/f$ noise component might exceed the white noise component up to several megahertz [4]. Furthermore, $1/f$ noise drastically increases as devices are scaled down to deep sub-micron size. Therefore, it is imperative to study and analyze $1/f$ noise in MOSFETs.

## 1.2 Literature review

In spite of extensive research and efforts to understand the low-frequency noise origin in semiconductor devices, there exists no unique theory to explain the low-frequency noise generation mechanism. Flicker noise in MOSFETs is usually perceived to be caused by carrier density fluctuations, which is the result of interaction of free carriers with oxide traps via interface states [2]. Several theories have been proposed to account for $1/f$ noise in MOSFETs, the most widely accepted being the number fluctuation model proposed by McWhorter based on tunneling transitions between traps in the oxide (called oxide traps) and channel carriers [5], [6], and the mobility fluctuation model [7 11], which is described by Hooge's empirical relation [7]. The number fluctuation ($\Delta N$) model and mobility fluctuation model ($\Delta\mu$), initially perceived to be mutually exclusive, have been used to explain the behaviors of $1/f$ noise. More research has led to the conclusion that both processes are present, but one of them dominates [12]. For long channel devices, it has been accepted that $\Delta N$ noise introduced by trapping and detrapping of channel carriers into defects dominates in NMOS transistors, and that bulk $\Delta\mu$ noise introduced by mobility scattering dominates in buried channel PMOS transistors [13 15]. As buried channel PMOS transistors have a channel at a larger distance from Si-$SiO_2$ interface, they are believed to be less noisy because of a lower probability of trapping and detrapping process than in surface channel NMOS transistors [15 17]. However, as devices are scaled down to deep sub-micron, buried channel PMOS transistors are forced to become a surface channel device to reduce the short channel

effects, such as drain-to-source leakage current. As a result, both NMOS and PMOS $1/f$ noise is now being governed by the same dominant noise generation mechanisms.

The McWhorter theory was proposed for low-frequency noise in germanium and assumes that origin of fluctuations is the tunneling of charge carriers at the semiconductor surface to and from traps, which are located close to the interface [2]. According to number fluctuation theory, the origin of flicker noise in MOSFETs is a surface phenomenon and is attributed to random trapping and detrapping processes of charges in the oxide traps near the Si-$SiO_2$ interface. The charge fluctuation results in fluctuation of the surface potential, which modulates the channel carrier density. The number fluctuation theory assumes that the channel can exchange charges with the oxide traps through tunneling. Extensive noise data have been reported, which support $\Delta N$ theory showing good correlation between flicker noise power and interface trap density [6, 18 20].

Opposite to the $\Delta N$ model is the so-called mobility fluctuation ($\Delta\mu$) theory, which considers mobility fluctuations as the origin of low-frequency noise, and for a homogenous semiconductor, assumes a volume and not a surface origin for this noise [7]. It is based on Hooge's relation for the spectral density of flicker noise and is purely empirical in nature. The mobility fluctuation theory proposes that the fluctuation of bulk mobility in MOSFETs is induced by fluctuations in phonon population through phonon scattering [9, 10]. Hooge and Vandamme's experiments on Ge and GaAs showed that only lattice phonon scattering gives $1/f$ noise [9]. Jindal and Zeil also showed that lattice phonon scattering is responsible for mobility fluctuation $1/f$ noise [10]. Later, they proposed a physically based mobility fluctuation model in 1981 [11]. According to this

model, the mobility fluctuation $1/f$ noise is caused by slow fluctuations in mean free path length of carriers.

To explain the low frequency noise in MOSFETs, the number fluctuation model has been predominantly used for NMOS and mobility fluctuation model has been used for PMOS. Some authors insist that the behavior of $1/f$ noise of both NMOS and PMOS can be explained by the number fluctuation model alone [21]. However, as devices are scaled down, these two models separated from each other cannot completely explain the low frequency noise as much more complicated physics are involved in the noise phenomena, including short channel effects [22], source/drain resistance [8, 23], quantum effects [24], RTS noise [25, 26], hot carrier effects [27, 28], and the correlation between number fluctuation and mobility fluctuation [25, 29]. Both the number fluctuation model and the mobility fluctuation model will be discussed in detail in **Chapter 2** (Section. 2.2). The inability of both the number fluctuation and mobility fluctuation models to completely explain the $1/f$ noise in MOSFETs can be understood by the fact that both of them are derived assuming only one prevailing noise source, whereas the drain current fluctuations are associated with drain conductance, which in turn is proportional to both carrier number and mobility. Surya *et al.* have combined the number and mobility fluctuation models, but treating those as uncorrelated [30]. As the carrier number fluctuation causes correlated mobility fluctuation by columbic scattering due to trapped oxide charges, the mobility and number fluctuations should be treated in a correlated manner [25, 29]. The unified flicker noise model for MOSFETs is based on correlation between carrier number fluctuation and mobility fluctuation with respect to fluctuation in trapped oxide charges [25].

## 1.3 Thesis contribution

This work is primarily an extension to the unified flicker noise model for MOSFETs. The unified flicker noise model [25] uses a semi-empirical fit to characterize the equivalent oxide-trap density represented by $N_t^*(E_{fn})$ that produces the same noise power if there is no contribution from mobility fluctuations. The three technology dependent parameters in the unified model are extracted from a global fit of the drain current noise characteristics measured in the strong inversion region. Celik *et al.* [31] proposed another empirical model to characterize oxide-trap energy distribution and subsequently low-frequency noise. In this work, the oxide-trap energy distribution is related with channel carrier number using Hooge's parameter, thus reducing the number of empirical constants to one as compared to three in the unified model.

As the MOSFET size scales down, the physical oxide thickness gets thinner, and the potential well under gate oxide splits the energy bands into subbands and causes quantum mechanical effects. Thus, the classical theory for calculation of charge under the gate is no longer accurate in sub-micron regime. As the devices under consideration in this work belong to the sub-micron regime, quantum mechanical calculations have been used instead of classical calculations.

Numerous effects have surfaced as a result of continuous scaling of MOSFETs to the nanometer range. New device architectures such as Silicon-On-Insulator (SOI) MOSFETs, Double Gate FETs (DGFETs), FinFETs, Tri-Gate FETs etc. are being devised to combat arising problems. More study is still needed for a deeper physics based understanding of noise behavior in nanoscaled electron devices. This work aims at

physics based modeling and characterization of nanoscaled non-conventional FETs, and extending the existing low frequency noise theory of MOSFETs to these structures. The model developed in this work is used to simulate three types of devices, which are single-gate (BULK) MOSFET, single-gate (SOI) MOSFET and double-gate (SOI) MOSFET. The steps followed in the modeling of low frequency noise are listed below:

1) Self-consistent solution of Schrödinger and Poisson equation to obtain charge under the gate with respect to gate voltage at Si-$SiO_2$ interface.
2) Implementing the charge control model obtained in previous step to devices under study.
3) *I-V* modeling of devices under study.
4) Modification of unified low frequency noise theory and implementation of model to devices under study.

### 1.4 Thesis organization

In **Chapter 2**, low frequency noise theory and its modeling have been described. The natures of the Si-$SiO_2$ interface and key factors which can affect $1/f$ noise of MOSFETs are discussed to provide the required background. The existing noise models based on number fluctuation, mobility fluctuation and the correlated fluctuation are described. In **Chapter 3**, the quantum mechanical model used to calculate inversion charge under the gate is described. **Chapter 4** discusses the *I-V* modeling of three different types of devices under study, namely single-gate (BULK) MOSFET, single- and double-gate (SOI) MOSFETs. In **Chapter 5**, the simulation results are presented and

analyzed. Finally, the work is summarized in **Chapter 6** and further necessary studies are suggested.

# *Chapter 2*
# Low frequency noise theory and modeling



## 2.1 Theory of low frequency noise

In order to study and analyze $1/f$ noise of MOSFETs, knowledge of the fundamental features of the Metal-Insulator-Semiconductor (MIS) system as well as the physical nature of electrons, holes, traps and interaction between carriers and the traps is needed. These traps and carriers are directly involved in the noise generation mechanisms such as trapping-detrapping and scattering. Specifically, the characteristics of traps in $SiO_2$ and at the Si-$SiO_2$ interface are important as they are directly related to the magnitude of $1/f$ noise of MOSFETs. Hence, it is critical to study the nature of the traps as well as their interaction with channel carriers, in order to understand the parameters affecting $1/f$ noise phenomenon.

There are four general types of charges associated with Si-$SiO_2$ system [32]. These are described below:

(1) Fixed oxide charge ($Q_f$, $N_f$): A positive charge, primarily due to structural defects in the oxide layer. The density of this charge, whose origin is related to the oxidation process, depends on oxidation ambient and temperature, cooling

conditions, and on silicon orientation. The fixed oxide charge does not interact with silicon layer.

(2) Mobile ionic charge ($Q_m$, $N_m$): These charges are due to ionic impurities such as $Li^+$, $Na^+$, $K^+$ etc. Negative ions and heavy metals may also contribute to this charge.

(3) Interface trapped charge ($Q_{it}$, $N_{it}$): These charges are located within the silicon forbidden gap at the Si-$SiO_2$ interface. Unlike a fixed oxide charge, an interface trapped charge reacts strongly with the underlying silicon and can thus be charged or discharged, depending on the surface potential. These types of charges are also called surface states, fast states and interface states.

(4) Oxide trapped charge ($Q_{ot}$, $N_{ot}$): These charges may be positive or negative as a result of a hole or an electron trapped in the bulk of the oxide. Trapping may result from ionizing radiation, avalanche injection, or other similar processes. The oxide trapped charges have generally been found to be positive, inducing negative charges in the silicon. Additionally, they communicate with the underlying silicon through trapping-detrapping processes. Unlike fixed oxide charge, this type of charge is generally annealed out by low temperature treatment, although neutral traps may remain.

The interface traps and oxide traps are involved in trapping-detrapping channel carriers (electrons for NMOS and holes for PMOS). From here on, interface traps and oxide traps will be used to represent the traps located at the Si-$SiO_2$ interface and in $SiO_2$, respectively. The interface traps are distinguished from oxide traps by their location, thus by their shorter relaxation time constants than those of the oxide traps.

Therefore, the interface traps contribute to relatively high frequency components of $1/f$ noise compared to the oxide traps whose time constants are longer that those of the interface traps and have a wide range of time constants, which are necessary to generate $1/f$ noise spectrum. In addition to their contribution to $1/f$ noise, both types of traps affect DC characteristics of MOSFETs [33]. The interface traps degrade the subthreshold slope and the oxide traps shift the threshold voltage.

The traps in the Si-$SiO_2$ system have been extensively studied. The techniques used include quasi-static C-V measurement [34], negative bias stress method [35], bias-temperature stress method [36], avalanche electron injection method [37], dual-transistor charge-pumping method [38], electron spin resonance technique [39], dual-transistor border trap charge separation method [40], irradiation and annealing technique [41], MIS conductance technique [42], and radiation method [43]. The interface traps are generally classified as donor-like or positive when empty and acceptor-like or negative when filled with an electron. The interface trap density strongly depends on the orientation of silicon due to different number of dangling bonds at the interface [42]. Application of a voltage across the Si-$SiO_2$ interface results in bending the energy bands near the interface. The potential in the silicon bulk is different from the potential at the interface, because of the band bending at Si-$SiO_2$ interface. The potential difference between the Si-$SiO_2$ interface and silicon bulk is defined as surface potential. The charge state of the interface traps is a strong function of the surface potential.

The oxide-traps are generally believed to be donor-like and the density of the oxide traps is independent of the oxide thickness and the surface potential, thus

applied gate bias [44]. This can possibly be used to explain typically observed higher $1/f$ noise for NMOS than PMOS as donor traps communicate more with electrons than with holes.

The other important physical factors that contribute to the low frequency noise generation mechanism are effective mobility fluctuation, potential barrier for electron or hole injection into an oxide film, and capture cross section of oxide traps [2]. The correlated models show that the *correlated* number and mobility fluctuation terms are proportional to effective mobility and the *pure* mobility fluctuation term is proportional to the square of the effective mobility of a hole or an electron [25]. One of the major reasons for higher $1/f$ noise in NMOS than PMOS transistors is the lower injection barrier for electrons than for holes to tunnel into an oxide film [41]. The value of potential barrier for electron injection into an oxide film is 3.1 eV, while corresponding value for a hole is 4.7 eV. The capture cross section of electron traps in oxide is larger ($10^{-12}$ $cm^2$) than that of a hole ($3 \times 10^{-13}$ $cm^2$), which makes it easier for the oxide traps to capture electrons than holes [45].

The existing models to explain the theory of low frequency noise in MOSFETs and their limitations are discussed in next section.

## 2.2 Existing models and their limitation

### 2.2.1 McWhorter number fluctuation model

McWhorter first proposed the number fluctuation model in 1957 [5]. Later, based on McWhorter's theory, many other authors have verified this noise mechanism. As

already explained in the previous section, McWhorter's number fluctuation model is based on the fluctuation in channel carrier density that is caused by random trapping and detrapping of oxide charges at Si-$SiO_2$ interface by oxide and interface traps. According to this model, low-frequency noise is proportional to the effective trap density, whose energy levels are located near the quasi-Fermi level of the inversion charge carriers. This has been verified through available experimental data [25]. The interface traps and oxide traps provide additional energy states. These states communicate randomly with the free charges in the channel. This mechanism obeys the Shockley-Read-Hall (SRH) statistics. By using these statistics, the mean square fluctuation of the number of trapped carriers in a volume $\Delta V = (Wdxdy)$ at a specific position is given by:

$$\Delta N_{trap} = \frac{4\tau}{1+\omega^2\tau^2} N_{trap} f_t (1-f_t) \Delta V \tag{2-1}$$

$\tau$ = trapping time constant (sec),

$N_{trap}$ = trap density per unit volume ($cm^{-3}$),

$f_t = [1+ \exp ( E_t - E_{fn}) / kT]^{-1}$ = probability of trap being filled by an electron under steady state condition,

k = Boltzmann constant (J/°K),

T = absolute temperature (°K),

$\omega = 2\pi f$, the angular frequency (rad/sec),

$E_t$ = trap energy level (eV), and

$E_{fn}$ = electron quasi-Fermi level (eV).

The fluctuation $\Delta N_t$ causes fluctuations in the channel free carriers $\Delta N$ that in turn cause fluctuation in the channel current. It is assumed that the channel can exchange charges with the oxide traps through tunneling. Although extensive experimental data

support this model, it fails to provide an adeuate explanation of the effect of correlated surface mobility fluctuation contribution to low-frequency noise.

### 2.2.2 Hooge mobility fluctuation model

In contrast to the number fluctuation model, the mobility fluctuation model considers the flicker noise as a result of fluctuation in bulk mobility [7, 8], based on Hooge's empirical relation for the spectral density of flicker noise in a homogeneous sample:

$$\frac{S_{I_D}}{I_D^2} = \frac{\alpha_H}{fN_{Total}} \tag{2-2}$$

where, $I_D$ is the mean current flowing through the sample, $S_{ID}$ is the noise current power spectral density, $f$ is the frequency, $N_{Total}$ is the total number of free carriers in the sample and $\alpha_H$ is Hooge's parameter. Hooge's mobility fluctuation model assumes a volume, not a surface, origin for low-frequency noise. As mentioned in Section. 1.2, this theory proposes that the fluctuation in bulk mobility is induced by phonon scattering. But in MOSFETs, other scattering mechanisms such as impurity scattering, surface roughness scattering, etc. exist. Thus, Hooge's parameter should be properly modified while calculating the low-frequency noise. The value of Hooge's parameter, $\alpha_H$, is found to have a universal value of about $2 \times 10^{-3}$ for homogenous silicon samples [2]. However, for MOSFETs, the value of Hooge's parameter was found to be one or several orders of magnitude smaller [25]. Also, the dependence of Hooge's parameter on the gate bias and oxide thickness has been observed [46], which contradicts Hooge's mobility fluctuation theory. The failure of Hooge's mobility fluctuation theory can be attributed to the fact that

(2-2) is only valid for homogenous devices. For a non-homogenous device, the differential form of the equation must be used.

### 2.2.3 Correlated low frequency noise model

Since neither the number fluctuation model nor the mobility fluctuation model was able to explain the low frequency noise generation mechanism completely, correlated models were introduced. Correlated low frequency noise models incorporate both number fluctuation and correlated surface mobility fluctuation. One such model is a simulation-oriented unified low frequency noise model, proposed by Hung et al. [25] based on the investigation of random telegraph noise in sub-micron MOSFETs. The study of random telegraph noise revealed that the charge fluctuations in the oxide traps generate noise by modulating the carrier mobility, in addition to the carrier number. The unified model incorporates both the number fluctuation and surface mobility fluctuation mechanisms. The surface mobility fluctuation is attributed to the Columbic scattering effect of the fluctuating oxide charges. The basis of correlation of number and mobility fluctuation is a common origin, which is oxide charge fluctuation. This model has a functional form resembling that based on the conventional number fluctuation model. But at certain bias conditions, the unified model can be reduced to the form compatible with bulk mobility fluctuation model. The calculation of Hooge's parameter value using unified noise model simulations shows same magnitude and bias dependence as reported experimentally [25, 46]. The limitation of the unified model is modeling of equivalent oxide trap density contributing to flicker noise using three technology dependent empirical fitting parameters. A global fit of the drain current noise characteristics measured in strong

inversion is used to extract the three empirical parameters that characterize the oxide trap energy distribution and mobility fluctuations.

### 2.3 This work – Modified correlated low frequency noise model

This work models the low-frequency noise in devices based on the unified flicker noise model, which incorporates both the number fluctuation and correlated surface mobility fluctuation mechanisms [25]. The random variation in the amount of trapped oxide charge introduces correlated channel carrier number and mobility fluctuations. The equivalent oxide trap density contributing to flicker noise is modeled in Hung *et al.*, using three technology dependent empirical fitting parameters, whereas this work correlates the equivalent oxide trap density near electron quasi-Fermi level with the inversion charge control of the device using the Hooge parameter.

A cross-section of the single-gate FET is shown in Fig. 2.1. Let $N$, $N_t$, $I_D$ and $\mu_{eff}$ be the number of channel carriers per unit area, the number of occupied traps per unit area, the drain current and the effective mobility, respectively.

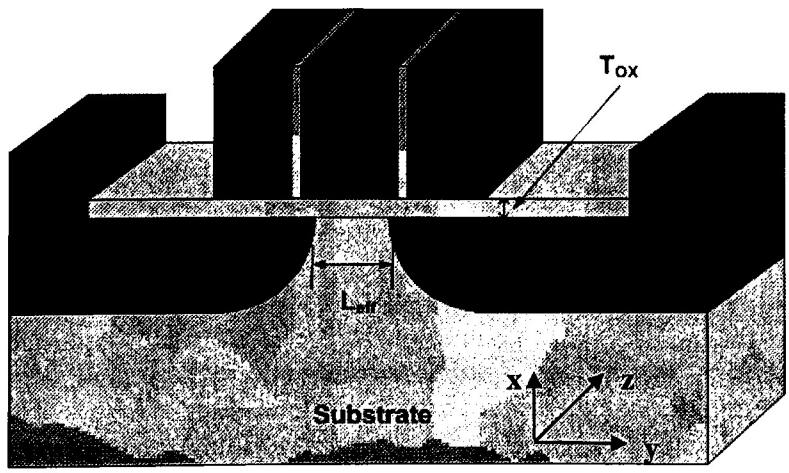


Fig. 2.1: Cross section of single-gate (BULK) MOSFET.

Let ($x$, $y$, z) be the coordinate system, where $x$ is in the direction perpendicular to the gate oxide with its origin at Si-$SiO_2$ interface, $y$ is in the direction of the length $L$, and $z$ is in the direction of the width $W$. Considering a section of the channel with width $W$ and length $\Delta y$, the resulting fractional change in the local drain current can be expressed as:

$$\frac{\partial I_D}{I_D} = \left[ \frac{1}{\Delta N} \frac{\partial \Delta N}{\partial \Delta N_t} + \frac{1}{\mu_{eff}} \frac{\partial \mu_{eff}}{\partial \Delta N_t} \right] \partial \Delta N_t \tag{2-3}$$

where, $\Delta N = NW\Delta y$ and $\Delta N_t = N_t W \Delta y$. The ratio of the fluctuations in the carrier number to fluctuations in the occupied trap number, $R$, is close to unity at strong inversion but assumes a smaller value at smaller bias conditions [47, 20]. A general expression for $R$ is [20]:

$$R = -\frac{\partial \Delta N}{\partial \Delta N_t} = -\frac{C_i}{C_{ox} + C_i + C_d + C_{it}} \tag{2-4}$$

where, $C_{ox}$, $C_i$, $C_d$, and $C_{it}$ are gate capacitance components associated with oxide layer, inversion layer, depletion layer, and interface traps, respectively.

The mobility model based on Matthiessen's rule is used to evaluate correlation of fluctuations in effective mobility to fluctuations in trapped oxide charges. Matthiessen's rule is given by:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_n} + \frac{1}{\mu_{ox}} = \frac{1}{\mu_n} + \alpha N_t \tag{2-5}$$

where, $\mu_n$ is the bulk carrier mobility that incorporates phonon scattering, impurity scattering, surface roughness scattering, $\mu_{ox}$ is the mobility limited by oxide charge

scattering [48] and $\alpha$ is the scattering coefficient (V-sec). Using $\Delta N_t = N_t W \Delta y$, simple mathematical analysis on the basis of (2-5) gives

$$\frac{\partial \mu_{eff}}{\partial \Delta N_t} = -\frac{\alpha \mu_{eff}^2}{W \Delta y} \tag{2-6}$$

Substituting (2-6) and (2-4) into (2-3) gives

$$\frac{\partial I_D}{I_D} = -\left(\frac{R}{N} + \alpha \mu_{eff}\right)\frac{\partial \Delta N_t}{W \Delta y} \tag{2-7}$$

The power spectrum density of the local current fluctuation is given as [25]:

$$S_{\Delta I_D}(y,f) = \left(\frac{I_D}{W \Delta y}\right)^2 \left(\frac{R}{N} + \alpha \mu_{eff}\right)^2 S_{\Delta N_t}(y,f) \tag{2-8}$$

where, $S_{\Delta N_t}(y,f)$ is the power spectral density of the mean square fluctuations in the number of the occupied traps over the area $W\Delta y$. According to the conventional theory of number fluctuations [2], $S_{\Delta N_t}$ is given by

$$S_{\Delta N_t}(y,f) = \int_{E_v}^{E_c} \int_0^W \int_0^{T_{ox}} 4N_t(E,x,y,z)\Delta y f_t(1-f_t) \cdot \frac{\tau(E,x,y,z)}{1+\omega^2\tau^2(E,x,y,z)} \Delta z \Delta x \Delta E \tag{2-9}$$

where, $N_t(E,x,y,z)$ is the distribution of the traps in the oxide and over the energy, $\tau(E,x,y,z)$ is the trapping time constant, $f_t = [1+ \exp(E_t - E_{fn}) / kT]^{-1}$ is the trap occupancy function, $E_{fn}$ is the electron quasi-Fermi level, $\omega = 2\pi f$ is the angular frequency, $T_{ox}$ is the oxide thickness, and $E_c - E_v$ is the silicon energy gap. Assuming that the probability of an electron penetrating into the oxide decreases exponentially with the distance from the interface, the trapping time constant is given by:

$$\tau = \tau_0(E)\exp(\gamma x) \tag{2-10}$$

where, $\tau_0(E)$ is the time constant at the interface and $\gamma$ is the attenuation coefficient of the electron wave function in the oxide [6]. For the Si-$SiO_2$ system the WKB theory for the carrier tunneling predicts that $\gamma = 10^8$ cm$^{-1}$ [25]. Assuming a uniform trap distribution for $0 < x < x_1$ and zero trap outside, which is true when $x_1$ is chosen such that traps for $x > x_1$ have a time constant $\tau$ that is so long that their effect on the noise cannot be measured, we have normalized distribution as:

$$\frac{\Delta x}{x_1} = \frac{\Delta \tau / \tau}{\ln(\tau_1 / \tau_0)} \tag{2-11}$$

for $\tau_0 < \tau < \tau_1$ and zero outside that interval [2], where $\tau_1$ is the time constant of trap at $x_1$. As the major contribution to noise will be from the traps around $E_{fn}$, and since $f_t(1-f_t)$ has a sharp peak at $E = E_{fn}$, using (2-10) and (2-11), the integral in (2-9) can be evaluated as:

$$S_{\Delta N_t}(y,f) = N_t(E_{fn})\frac{kTW\Delta y}{\gamma f} \tag{2-12}$$

Detailed derivation of (2-12) is provided in the Appendix. The total drain current noise power is given by [2]:

$$S_{I_D}(f) = \frac{1}{L^2}\int_0^L F(y,f)\,dy \tag{2-13}$$

where, $L$ is the gate length, $F(y,f) = S_{\Delta I_D}(y,f)\Delta y$ and $S_{\Delta I_D}(y,f)$ is the spectrum of the primary current fluctuation in the section $\Delta y$ at $y$. Substituting (2-12) into (2-8), and evaluating (2-13) we get (see Appendix):

$$S_{I_D}(f) = \frac{kTI_D^2}{\gamma f WL^2}\int_0^L N_t(E_{fn})\left[\frac{R}{N} + \alpha\mu_{eff}\right]^2 dy$$

$$= \frac{kTqI_D\mu_{eff}}{\gamma f L^2}\int_0^{V_D} N_t(E_{fn})\left(1+\alpha\mu_{eff}NR^{-1}\right)^2\frac{R^2}{N}dV \tag{2-14}$$

The only unknown in the above equation is $N_t(E_{fn})$, for which various low-frequency noise models use an empirical fit to match the experimental noise data. The equivalent oxide-trap density is characterized using three technology dependent empirical parameters extracted from a global fit of the drain current noise characteristics in the unified low frequency noise model [25]. In this work, the oxide-trap energy distribution is related to channel carrier number using Hooge's parameter. According to Klassen's theory of low frequency noise [49], the power spectral density of the mean square fluctuations in the number of occupied traps per unit area is given as:

$$S_{\Delta N_t}(y,f) = \frac{\alpha_H \Delta N}{f} \tag{2-15}$$

where $\alpha_H$ is Hooge's parameter. Equating (2-15) with (2-12), we have:

$$\frac{\alpha_H \Delta N}{f} = \frac{N_t(E_{fn}) kTW\Delta y}{\gamma f} \tag{2-16}$$

For MOSFETs in the strong inversion region:

$$\frac{q\Delta N}{\Delta y} = C_{ox} W\left(V_{GS} - V_{TH} - V(y)\right) \tag{2-17}$$

where, $V_{GS}$ is applied gate-to-source voltage, $V_{TH}$ is threshold voltage of the device, and $V(y)$ is the potential varying along the channel on application of voltage at drain. Substituting (2-17) into (2-16), we have:

$$\frac{N_t(E_{fn})kT}{\gamma} = \frac{\alpha_H C_{ox}\left(V_{GS} - V_{TH} - V(y)\right)}{q} \tag{2-18}$$

The above equation shows the dependence of oxide-trap energy distribution on channel charge and applied bias, a result which is experimentally verified [50].

In this work, with accurate quantum mechanical modeling of channel charge, the above relationship has been used to calculate the resultant drain current noise power spectrum integral in (2-14). The drain current has been modeled based on the analytical models presented in **Chapter 4.** The results of quantum analysis, *I-V* modeling and low frequency noise calculation are presented and discussed in **Chapter 5.**

*Chapter 3*

# Quantum Mechanical Modeling



## 3.1 Introduction

Modern silicon technology has already been pushed well into the submicron regime, now approaching at a laboratory level the nanometer feature size. Under such conditions, quantum effects in the inverted channel of MOSFETs become important and strongly influence the device behavior and performance.

In a p-type semiconductor, when the energy bands near the surface are bent down enough that the conduction band lies near or below the Fermi level, an n-type inversion layer is formed. This band bending can be introduced by the presence of positive charges at or near the surface associated with impurity ions or other Coulomb centers, or by applying an electric field to the surface [51]. As the devices are continually scaled down to smaller dimensions, accurate inversion charge modeling has become very important for modeling their electrical characteristics.

The following different techniques have been used for the evaluation of charge density in the inversion layer [52]:

1) The simplest technique, often referred to as the classical inversion charge control model in literature, assumes that the inversion charge depends linearly on gate voltage in strong inversion. This model considers the inversion layer charge as a sheet charge and overestimates the inversion charge density at the Si-$SiO_2$ interface. The model is based on Maxwell-Boltzman and Fermi-Dirac statistics. The limitations of this model are discussed in next section.
2) Another technique is deriving the inversion charge directly from gate-channel capacitance measurements through numerical integration. This method is referred to as the split *C-V* method. This is an experimental way of measuring inversion charge density, and depends heavily on sensitivity and accuracy of instruments used.
3) Another way of obtaining inversion charge density is solving the Poisson- Schrödinger equations self-consistently. This technique, referred to as quantum mechanical modeling, accounts for finite inversion charge thickness, energy level quantization at Si-$SiO_2$ interface in MOS structures, and predicts the inversion charge carrier density accurately. The details of quantum mechanical modeling are discussed in Section. 3.3.

### 3.2 Limitations of classical charge control model

In the classical model, the electrons induced at the semiconductor-insulator interface of a MOSFET form a classical electron gas and behave essentially in the same way as electrons in a bulk semiconductor [53]. This assumption is valid only if the thickness of the inversion layer is much larger than the deBroglie wavelength. In the

scaled-down MOSFETs, with oxide thickness reaching well below 100 Å, the inversion layer thickness may become smaller than the deBroglie wavelength. In such a scenario, inversion carriers in the inversion layer are confined in the potential well very close to the silicon surface and should be treated quantum-mechanically as a two-dimensional gas, especially at high normal fields. The energy levels of electrons are grouped in discrete subbands, each of which corresponds to a quantized level for motion in the normal direction [54]. If the electrons are represented as wavefunctions, then the nature of the electron distribution in the inversion-layer differs significantly from the case in which the electrons are treated as classical particles, as shown in Fig. 3.1 below (not to scale).

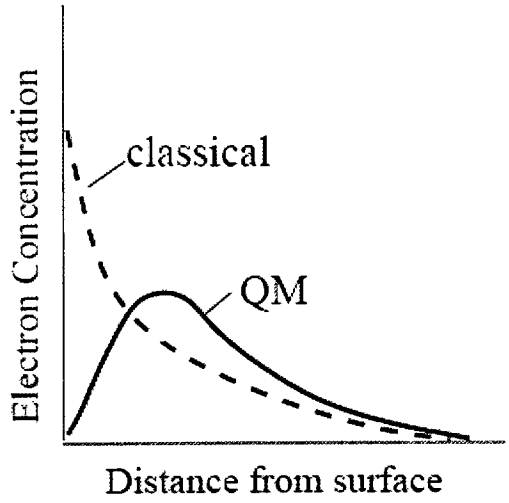


Fig. 3.1: Electron distribution (not to scale) using classical and quantum-mechanical model.

The classical model fails to take into account the quantization of energy levels in the potential well at the semiconductor-insulator interface in the direction perpendicular to the $Si\text{-}SiO_2$ interface for accurate calculation of inversion charge.

### 3.3 Quantum mechanical model

As devices shrink to nanometer scales, their dimensions begin to approach the wavelength of the electron. The operation of deep-submicron MOSFETs is now entering a regime in which quantum-mechanical effects become noticeable and classical physics is no longer sufficient for accurate modeling of operating characteristics. The finite thickness of the inversion layer, mostly due to quantum-mechanical effects, not only causes a discrepancy between the oxide capacitance and the measured capacitance but also degrades the transconductance [55, 56]. It has been shown that the inversion charge density calculated quantum-mechanically is smaller than that calculated classically for a given gate voltage, thus affecting the shift of the subthreshold curves [57]. Therefore, the inversion charge carrier density must be accurately calculated using the quantum mechanical model to better understand device physics and modeling. Since the pioneering research by Stern and Howard [51] to model inversion charge carrier by solving the Poisson- Schrödinger equations self-consistently, a number of articles concerning the self-consistent solution of Poisson- Schrödinger equations have been published and research on this subject is still being carried out.

In this work, inversion layer charge in single- and double-gate devices is calculated by solving Poisson and Schrödinger equations self-consistently to incorporate the effect of energy level quantization at the interface. When energy bands are bent strongly near a semiconductor-insulator interface, the potential well formed by the interface barrier and the electrostatic potential in the semiconductor can be narrow enough that quantum-mechanical effects become important. Only a given carrier type is treated quantum-mechanically when confined by the surface potential. When electrons

are confined, the electrical characteristics of an MOS structure are modeled by solving the coupled effective-mass Schrödinger and Poisson equations self-consistently [58]:

$$-\frac{\hbar^2}{2m^*}\frac{\partial^2}{\partial x^2}\psi(x)+V(x)\psi(x)=E\psi(x) \tag{3-1}$$

where, $x$-direction is given by direction perpendicular to interface and going into substrate,

$\hbar$ = modified Planck's constant,

$\Psi(x)$ = electron wave function

$m^*$ = effective mass of an electron,

$V(x)$ = varying potential along the x-direction,

$E$ = electron energy (eV)

and

$$\frac{d^2V}{dx^2}=-\frac{q}{\varepsilon(x)}\left[-n-N_A+p+N_D\right] \tag{3-2}$$

where, $N_A$ is the substrate doping concentration,

$\varepsilon(x)$ is the permittivity of the material along x-direction.

The wave function $\psi(x)$ in (3-1) and the electron density $n(x)$ (Si and $SiO_2$ regions) in (3-2) are related by using Fermi-Dirac statistics:

$$n(x)=\frac{kT}{\pi\hbar^2}\sum_i g_i m^*_i \sum_j \ln\left[1+\exp\left(\frac{(E_{fn}-E(j))}{kT}\right)\right]|\psi_{i,j}(x)|^2 \tag{3-3}$$

where, j = number of eigen states,

$E_{fn}$ = electron quasi-Fermi energy,

$E(i)$ = electron eigen energy,

and $g_i$ and $m^*_i$ are the ith valley degeneracy and the ith density-of-states effective mass, respectively. To find the eigenfunctions and eigenenergies of an electron, Schrödinger's (3-1) and Poisson's equations (3-2) have to be solved self-consistently.

In this work, inversion layer charge in bulk and SOI MOSFETs has been modeled using the above system of equations. The interaction between the front and back inversion layers in double-gate SOI devices has been studied as a function of the silicon film thickness and electron concentration. The quantum mechanical model has been used to calculate the threshold voltage as explained in Section. 4.2.

*Chapter 4*

# Devices and their $I - V$ modeling



## 4.1 Types of MOSFETs under study

Much work has already been done on transistor scaling limits [59] and on the role of non-equilibrium carrier transport [60]. Continuous scaling of MOSFETs to the nanometer range gives rise to numerous short-channel effects such as drain induced barrier lowering, punchthrough, velocity saturation, hot electron effects, etc., which are not observed in long-channel transistors. In order to face the arising problems, new device architectures such as Silicon-On-Insulator (SOI) MOSFETs, Double Gate FETs (DGFETs), FinFETs, Tri-Gate FETs, etc. are being devised, which are more effective in preventing short-channel effects. Hitherto, little attention has been paid to noise properties, and much work is still needed for a deeper physics-based understanding of noise behavior in nanoscaled electron devices. This work aims at physics-based modeling and characterization of nanoscaled non-conventional FETs, and extending the existing low frequency noise theory of MOSFETs to these structures.

The model developed in this work is used to simulate three types of devices, which are the single-gate (BULK) MOSFET, single-gate (SOI) MOSFET and double-gate (SOI) MOSFET.

## 4.2 Threshold voltage calculation

To calculate the threshold voltage of the device, the unified charge control model (UCCM) has been used [61]. The unified charge control model is based on quantum mechanical formulation of the two-dimensional electron gas (2DEG) formed in silicon inversion layers. It gives the relationship to calculate inversion charge density, $n_{inv}$ as a function of gate-to-source voltage, $V_{GS}$ for a given oxide thickness. The unified charge control model for an n-channel MOSFET is given as:

$$V_{GS} - V_{TH} = \eta V_T \ln \frac{n_{inv}}{n_0} + a\left(n_{inv} - n_0\right) \tag{4-1}$$

where

$$a = q\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{\Delta d}{\varepsilon_{Si}}\right) = q\left(\frac{1}{C_{ox}} + \frac{1}{C_{inv}}\right) \tag{4-2}$$

$V_{GS}$ = applied gate-to-source voltage,

$V_{TH}$ = threshold voltage,

$\eta$ = ideality factor related to subthreshold characteristics,

$V_T$ = thermal voltage,

$q$ = electron charge,

$\varepsilon_{ox}$ = permittivity of silicon dioxide,

$\varepsilon_{Si}$ = permittivity of silicon,

$n_o = \frac{C_{ox}\eta V_T}{2q}$, the sheet charge density at threshold voltage derived later in this section,

$\Delta d$ = effective width of 2DEG at strong inversion.

The value of $\Delta d$ for an n-channel device with substrate doping of $1 \times 10^{17}$ $cm^{-3}$ is of the order of 11 ´ [61]. As the value of $\Delta d$ is negligible as compared to oxide thickness of the device, the term $\Delta d/\varepsilon_{Si}$ is very small as compared to $t_{ox}/\varepsilon_{ox}$. Rearranging (4-1) and taking its derivative with respect to $V_{GS}$ to find gate-to-channel capacitance:

$$C_{gc} = q\frac{dn_{inv}}{dV_{GS}} = \frac{qn_{inv}}{\eta V_T + an_{inv}} \tag{4-3}$$

where $C_{gc}$ is the gate-to-channel capacitance calculated using the quantum mechanical model. Taking the second derivative of (4-1) with respect to $V_{GS}$:

$$\frac{dC_{gc}}{dV_{GS}} = q\frac{d^2 n_{inv}}{dV_{GS}^2} = q\frac{(\eta V_T n_{inv})}{(\eta V_T + an_{inv})^3} \tag{4-4}$$

It can be deduced by equating the derivative of (4-4) to zero that it reaches its maximum value at:

$$n_{inv} = \frac{\eta V_T}{2a} \tag{4-5}$$

Defining the threshold voltage as the point where (4-4) reaches its maximum value leads to:

$$n_{inv}\,|_{V_{GS}=V_{TH}} = n_0 = \frac{\eta V_T}{2a},\ and\ C_{gc}\,|_{V_{GS}=V_{TH}} = \frac{q}{3a} = \frac{C_{gc,\max}}{3} \tag{4-6}$$

In other words, the threshold voltage of the device can be defined as the point where the gate-to-channel capacitance is one third of the maximum gate-to-channel capacitance $C_{gc,max}$, which is the same as the oxide capacitance.

### 4.3 *I-V* modeling of single-gate (Bulk) MOSFET

A short channel MOSFET model based on pseudo-two dimensional analysis for the drain region is used in this work [62] to model *I-V* characteristics of single-gate MOSFET. The model incorporates second order effects such as mobility degradation, velocity saturation, and short channel effects such as channel length modulation. The model takes into account the dependence of electrical characteristics on processing parameters. With continuous channel length scaling, the maximum channel electric field is increasing. Most of the *I-V* models in literature are based on the two-section approach, which consists of dividing the channel length into two regions, namely low-field and high-field region [32]. The gradual channel approximation is used in the region extending from the source to the point of saturation.

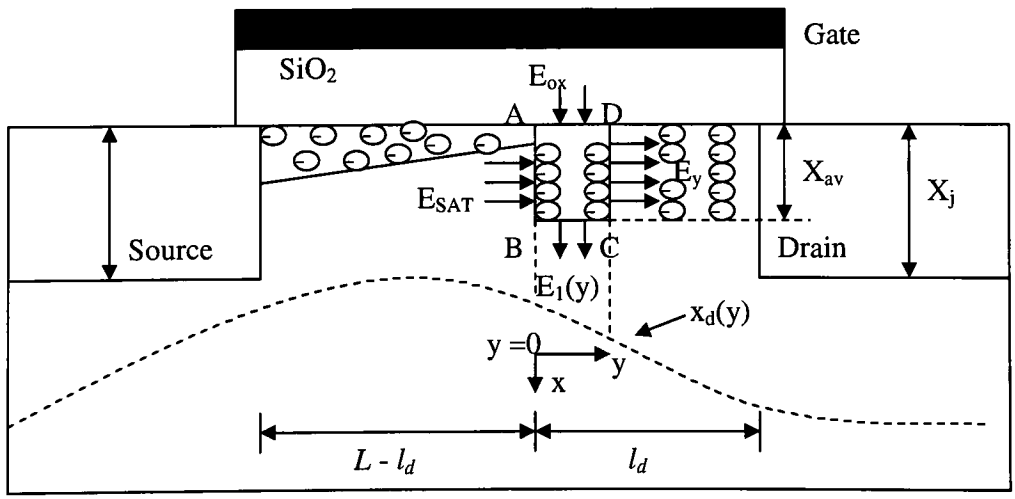


Fig. 4.1: Cross section of single-gate MOSFET showing source, drain region and Gaussian surface (ABCD) [62].

In the drain region having length $l_d$ as shown in Fig. 4.1, beyond the point of saturation the gradual channel approximation fails and a two-dimensional (2D) approach is needed to solve the problem.

In the literature, there are several analytical approaches used to find $l_d$ and the channel field in the drain region. These approaches can be classified into two major categories:

1) Constant field gradient approximation.
2) Quasi 2-D approximation.

Constant field gradient approximation assumes the gradient of the channel field to be constant and is based on solution of the 1-D Poisson's equation. Although the models based on constant field gradient approximation are simple, it fails to provide exact analysis of channel field in the vicinity of the drain region.

The models based on a quasi 2-D approximation select a Gaussian surface, accounting for the charge in the drain region and Gauss's law is applied to the surface sides [63]. A second-order differential equation in the channel potential is obtained, which is solved according to the given boundary conditions to yield the channel potential and channel lateral field inside the drain region. Most models assume a rectangular box for the Gaussian surface. The depth of the rectangle is assumed equal to the depletion region depth at the point of saturation in El-Mansy model [63]. In the unified model [62], the depth of rectangular Gaussian box is assumed constant relative to drain junction depth. The model used in this work is based on pseudo-2D analysis of a rectangular Gaussian surface in the drain region of depth $X_{av}$, as shown in Fig. 4.1. As already mentioned earlier, the analysis incorporates the electrical characteristics' dependence on

device processing parameters such as junction depth, oxide thickness, channel width, channel length and doping profile.

In linear mode of operation, the drain current of MOS transistor is given by:

$$I_{DL} = W \mid Q_n(y) \mid v(y) \tag{4-7}$$

where, W is the width of the channel, $Q_n$ is the inversion layer charge per unit area under the gate and $v(y)$ is the drift velocity. Introducing a geometrical factor $F$ [64] to account for short channel effects and using the gradual channel approximation, the inversion charge layer can be written as:

$$Q_n(y) = C_{ox}\left[V'_G - V(y) - K_1 F\sqrt{2\psi_B + V_{SB} + V(y)}\right] \tag{4-8}$$

where

$$V'_G = V_G - 2\psi_B - V_{FB}, \text{ and } K_1 = \sqrt{2\varepsilon_s q N_A}/C_{ox} \tag{4-9}$$

$C_{ox}$ is the oxide capacitance per unit area, $V_{FB}$ is the flat band voltage, $V_{SB}$ is the substrate voltage and $\psi_B$ is the fermi-potential. With a Taylor's expansion around $V(y) = 0$, and retaining two terms of the expansion, $Q_n(y)$ is expressed as:

$$Q_n(y) = C_{ox}\left[V_G - V_T - 2a_0 V(y)\right], \tag{4-10}$$

where

$$2a_0 = 1 + K_1 F / 2\sqrt{2\psi_B + V_{SB}} \text{ and } V_T = 2\psi_B + V_{FB} + K_1 F\sqrt{2\psi_B + V_{SB}} \tag{4-11}$$

Due to the combined action of the normal electric field at Si-$SiO_2$ interface and the lateral electric field, the mobility of electrons in the inversion layer is less than the bulk. The surface mobility dependence on the both the lateral and vertical field is expressed by:

$$\mu = \frac{\mu_0}{1 + \theta_m(V_{GS} - V_{TH})}\frac{1}{1 + E(y)/E_c} \tag{4-12}$$

where $\mu_o$ is the low field mobility, $\theta_m$ is empirically determined and is inversely proportional to the oxide thickness [32]. The field $E_c$ is a varying parameter used to calculate the lateral field at the transition point. Using (4-7) (4-12) and integrating over the channel length $L$, the drain current expression in the linear region of operation is given as:

$$I_{DL} = W\mu_{eff}C_{ox}\frac{(V_{GS} - V_{TH} - a_0 V_{DS})V_{DS}}{L(1+V_{DS}/LE_c)} \tag{4-13}$$

where

$$\mu_{eff} = \frac{\mu_0}{1+\theta_m(V_{GS} - V_{TH})} \tag{4-14}$$

At the drain end of the region, the drain voltage $V_{DSAT}$ at which the charge carriers reach their high field limiting velocity, $v_{SAT}$ defines the transition from the linear to the saturation region. At drain voltages higher that $V_{DSAT}$, the interface between high and low field regions along the channel moves toward the source, resulting in the channel length modulation effect. As mentioned earlier, a two-section approach is used to model the saturation region of operation. The drain current in the saturation region is given by (4-13), except that the effective channel length is $L$-$l_d$, and $V_{DS}$ is replaced by $V_{DSAT}$. The drain current is given by:

$$I_{DS} = \frac{I_{DSAT}}{1 - l_d/L_{eq}} \tag{4-15}$$

where

$L_{eq} = L(1+V_{DSAT}/LE_c)$ and $I_{DSAT} = I_{DL}|_{V_{DS}=V_{DSAT}}$. To evaluate (4-15), determination of both the length of the high field region $l_d$, and the saturation voltage $V_{DSAT}$ is required. Also, the lateral field at transition point is unknown. This is in contradiction with the use

of a piecewise linear velocity-field relationship [62], which defines the saturation field by $E_c$. It is assumed that in the drain region, the mobile electrons are spread over an average depth given by $X_{av} = (X_1 + X_j)/2$, where $X_1$ is the depletion region depth at the transition point and $X_j$ is the drain junction depth, as shown in Fig. 4.1. Applying Gauss's law to the rectangle ABCD in Fig. 4.1,

$$-\int_0^{X_{av}} \varepsilon_s E_{SAT}\,dx + \int_0^{y} \varepsilon_s E_1(y)\,dy + \int_0^{X_{av}} \varepsilon_s E(y)\,dx - \int_0^{y} \varepsilon_{ox} E_{ox}\,dy = -q\int_0^{y}\left[\int_0^{X_{av}} (n + N_A)\,dx\right]dy \quad (4\text{-}16)$$

where $E_{SAT}$, $E_{ox}$, $E_1(y)$ and $E(y)$ are the electric fields perpendicular to the boundaries AB, AD, BC and CD respectively. $E_1(y)$ is found by solving the 1-D Poisson's equation:

$$\frac{\partial^2 \psi}{\partial x^2} = \frac{qN_A}{\varepsilon_s} \quad (4\text{-}17)$$

subject to the boundary conditions, $\psi = \frac{d\psi}{dx} = 0$ at $x = x_d(y)$. With an assumption that the depletion layer boundary in the drain region varies linearly with the lateral dimension, which is $x_d(y) = ky + X_1$, where the slope, $k = (W_D - X_1)/l_d$ and $W_D$ is the depletion layer depth at the drain junction, $E_1(y)$ can be expressed as:

$$E_1(y) = \frac{qN_A}{\varepsilon_s}\left[ky + X_1 - X_{av}\right] \quad (4\text{-}18)$$

The mobile charge density, $Q_m$ in the drain region can be given as:

$$Q_m = -q\int_0^{X_{av}} n\,dx = \frac{-I_{DSAT}}{wv(E_{SAT})} \quad (4\text{-}19)$$

Differentiating (4-16) with respect to $y$, and combining with (4-18) and (4-19) gives:

$$qN_A X_1 + qN_A ky + \varepsilon_s X_{av}\frac{dE_y}{dy} - \frac{\varepsilon_{ox}}{t_{ox}}(V_G' - V(y)) = \frac{-I_{DSAT}}{Wv(E_{SAT})} \quad (4\text{-}20)$$

Also, in strong inversion the channel charge can be given by:

$$qN_A X_1 \approx C_{ox}\left(V_G - V_{DSAT}\right) \tag{4-21}$$

Substituting (4-21) into (4-20) and using $dE(y)/dy = -d^2V(y)/dy^2$ gives:

$$\frac{d^2V(y)}{dy^2} - A^2\left(V(y) - V_{DSAT}\right) = \kappa A^2 y + C \tag{4-22}$$

where

$A^2 = C_{ox} / X_{av}\varepsilon_s$,

$C = I_{DSAT} / X_{av}\varepsilon_s W v(E_{SAT})$, and

$$\kappa = \frac{kqN_A}{C_{ox}}$$

Applying boundary conditions:

at $y = 0$, $V(y) = V_{DSAT}$ and $E(y) = E_{SAT}$ and solving (4-22) gives [62]:

$$V(y) = V_{DSAT} + \left(C/A^2\right)\left(\cosh(Ay) - 1\right) + (1/A)\left(|E_{SAT}| + \kappa\right)\sinh(Ay) - \kappa y \tag{4-23}$$

and,

$$|E(y)| = |E_{SAT}|\cosh(Ay) + \kappa\left(\cosh(Ay) - 1\right) + (C/A)\sinh(Ay) \tag{4-24}$$

At the drain end, using (4-23) gives:

$$V_{DS} = V_{DSAT} + \left(C/A^2\right)\left(\cosh(Al_d) - 1\right) + (1/A)\left(|E_{SAT}| + \kappa\right)\sinh(Al_d) - \kappa l_d \tag{4-25}$$

(4-25) can be used to compute $l_d$. Using (4-7), (4-10) and (4-13), an additional equation relating $V_{DSAT}$ and $E_{SAT}$ can be obtained as (see Appendix):

$$a_0 V_{DSAT} E_{SAT}\left(L + V_{DSAT}/E_c\right) + \left(V_G - V_T - a_0 V_{DSAT}\right)\left(V_{DSAT} - LE_{SAT} - \frac{E_{SAT}V_{DSAT}}{E_C}\right) = 0 \tag{4-26}$$

Also, using (4-13) and (4-15) gives [62]:

$$|E_{SAT}|^3 / E_{01}^2 + |E_{SAT}| - E_{02}/2 = 0 \tag{4-27}$$

where

$$E_{01} = \frac{1}{L}\sqrt{\frac{(V_G - V_T - a_0 V_{DSAT})V_{DSAT}}{a_0 + (V_G - V_T)/LE_c}}, \text{ and } E_{02} = CL_{eq}.$$

(4-25), (4-26) and (4-27) form a system of equations that can be solved numerically for a given gate voltage $V_G$ to find the saturation voltage $V_{DSAT}$, the channel field at saturation $E_{SAT}$ and the drain region length $l_d$. These values can be then used to get the $I_{DS}$ $V_{DS}$ characteristics. A submicron ($L$ = 0.25 μm single-gate MOSFET was simulated and verified with experimental data using this model. The results are presented in **Chapter 5.**

### 4.4 *I-V* modeling of single- and double- gate SOI MOSFET

As MOSFET scaling aggressively continues down to the sub-50 nm scale, single- and double-gate (DG) devices on SOI substrates are likely to replace conventional bulk devices [65]. The advantage of SOI devices are higher current drive, higher transconductance, and smaller subthreshold swing as compared to bulk devices. Cross-sections of single- and double-gate SOI MOSFET are shown in Fig. 4.2a and 4.2b, respectively.

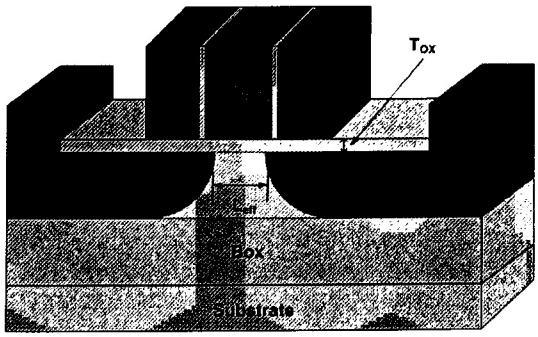


Fig. 4.2a: Cross section of single-gate SOI MOSFET

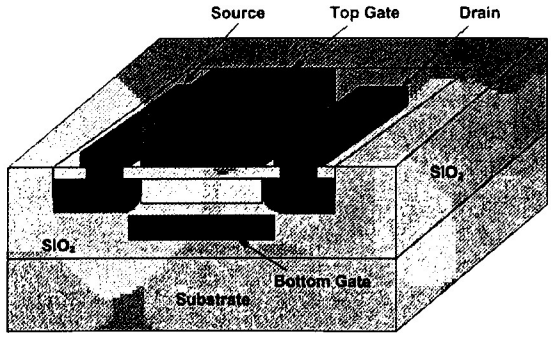


Fig. 4.2b: Cross section of double-gate SOI MOSFET

A comprehensive, physically representative charge-based model for the small geometry enhancement-mode MOSFET fabricated in thin SOI films is used in this work to model electrical characteristics [66]. The model accounts for the predominant short-channel effects such as threshold voltage reduction due to charge sharing, channel-conductivity enhancement due to drain bias, field-dependent carrier velocity including velocity saturation and mobility degradation, and channel length modulation. Fig. 4.3 shows a cross-sectional view of a generic n-channel SOI MOSFET.

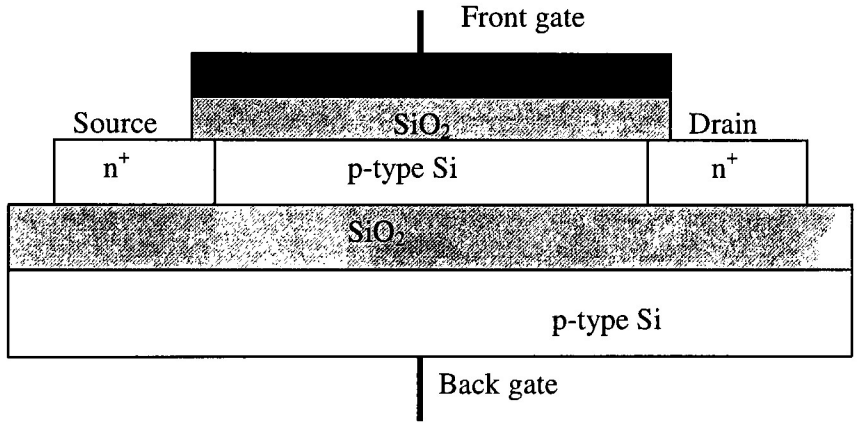


Fig. 4.3: Cross-sectional view of generic n-channel SOI MOSFET.

In short-channel bulk MOSFETs, the threshold voltage defined for low drain-source voltage is reduced due to depletion charge sharing by the source and drain under the gate [32]. In the SOI device, the coupling between the front and back gates influences this charge sharing. The thin film is assumed to be completely depleted in strong inversion, except for sheets of surface charge $Q_{cf0}$ and $Q_{cb0}$ at the front and back surfaces, respectively. (The subscripts *f* and *b* refer to the front and back surfaces, and the subscript 0 refers to the solution for zero drain-source voltage.) The potential of the front surface,

$\psi_{sf0}$ is approximately constant between the source and drain, equal to twice the Fermi potential of the neutral film, to which all potentials are referred. At the back interface, the potential varies from the junction built-in potential ($V_{bi}$) in the source and drain regions, to a surface potential $\psi_{sb0}$ mid-way between the source and drain. The depletion charge associated with gate, source and drain may be regionally divided into three portions as shown in Fig. 4.4.

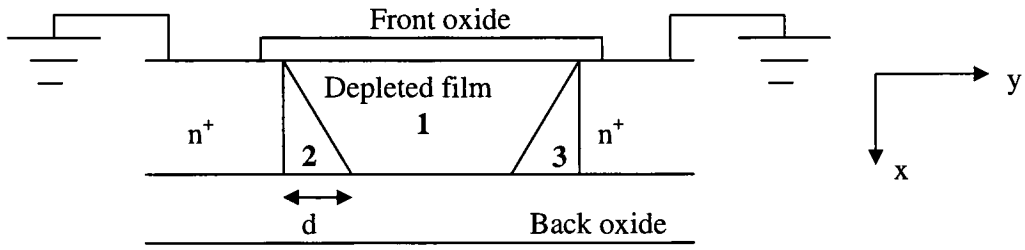


Fig. 4.4: Cross-sectional view of SOI MOSFET showing completely depleted film and the regions 1, 2, and 3 controlled by gates, source and drain respectively [66].

The first portion is defined by a trapezoid and the effective depletion charge per unit area controlled by the gates is given as:

$$Q_{b(eff)} = -qN_A t_b (1 - d/L) \approx Q_b (1 - d/L) \tag{4-28}$$

where, $Q_b$ equals -q$N_A t_b$ and $t_b$ is the film thickness. From [67], under the condition that drain-to-source voltage, $V_{DS}$, is zero, replacing $Q_b$ by $Q_{b(eff)}$ gives:

$$Q_{cf0} = -C_{of}\left[V_{GfS} - V_{FB}^{f} - \left(1 + \frac{C_b}{C_{of}}\right)\psi_{sf0} + \frac{C_b}{C_{of}}\psi_{sb0} + \frac{Q_{b(eff)}}{2C_{of}}\right] \tag{4-29}$$

and,

$$Q_{cb0} = -C_{ob}\left[V_{GbS} - V_{FB}^{b} - \left(1 + \frac{C_b}{C_{ob}}\right)\psi_{sb0} + \frac{C_b}{C_{ob}}\psi_{sf0} + \frac{Q_{b(eff)}}{2C_{ob}}\right] \tag{4-30}$$

where,

$C_b = \varepsilon_s / t_b, C_{of} = \varepsilon_{ox} / t_{of}, C_{of} = \varepsilon_{ox} / t_{ob}$ are the front and back oxide capacitances per unit area and $V^f_{FB}$ and $V^b_{FB}$ are the front- and back-gate flat-band voltages. $V_{GfS}$ and $V_{GbS}$ are the applied front and back bias voltages.

The effective lateral component of the electric field $E_{b(eff)}$ at the back interface in the model is approximated as [67]:

$$E_{b(eff)} = \left[qN_A\left(V_{bi} - \psi_{sb0}\right)/2\varepsilon_s\right]^{1/2} + f_\alpha \frac{\varepsilon_{ox}}{\varepsilon_s}\frac{\left(V_{GbS} - V^b_{FB} - \psi_{sb0}\right)}{t_{ob}} + f_\beta \frac{\varepsilon_{ox}}{\varepsilon_s}\frac{\left(V_{bi} - V_{GbS} + V^b_{FB}\right)}{t_{ob}} \tag{4-31}$$

where the depletion charge results in the first term and the second and third terms are due to fringing fields from region 1 and from the source to the back gate. The terms, $f_\alpha$ and $f_\beta$ are empirical parameters [67]. The term, d in (4-28) can be now analytically approximated as:

$$d \approx \left(V_{bi} - \psi_{sbo}\right) / E_{b(eff)} \tag{4-32}$$

With the application of $V_{DS}$, the channel charge is modulated indirectly through the two-dimensional Poisson equation in the film and directly through the gradient induced in surface potential along the channel. The model used in this work is based on $V_{DS}$-induced change in the channel charge, $\Delta Q_{cf}$ [66]. The potentials $\psi(x, y)$, $\psi_{sf}(y)$ and $\psi_{sb}(y)$ as well as charges $Q_{cf}(y)$ and $Q_{cb}(y)$ change by amounts $\Delta\psi(x, y)$, $\Delta\psi_{sf}(y)$, $\Delta\psi_{sb}(y)$, $\Delta Q_{cf}(y)$ and $\Delta Q_{cb}(y)$, respectively, on application of $V_{DS}$.

Writing Laplace's equation for incremental channel potential gives:

$$\frac{\partial^2(\Delta\psi)}{\partial x^2} + \frac{\partial^2(\Delta\psi)}{\partial y^2} = 0 \tag{4-33}$$

The boundary conditions for (4-33) are:

$$\Delta\psi(x,0)=0,\Delta\psi(x,L)=V_{DS},\Delta\psi(0,y)=\Delta\psi_{sf}(y),\Delta\psi(t_b,y)=\Delta\psi_{sb}(y) \tag{4-34}$$

Assuming that the two partial derivatives are not strongly coupled in (4-33) to obtain the closed form solution, and extrapolating for long channel case for which each term is zero [66]:

$$\frac{\partial^2(\Delta\psi)}{\partial x^2}=-\frac{\partial^2(\Delta\psi)}{\partial y^2}=-\eta \tag{4-35}$$

where, $\eta$ is an empirical constant, which approaches zero as $L$ increases. Integrating (4-35) for the limit $y = 0$ to $y = L$:

$$\eta=\left(2/L^2\right)\left[V_{DS}+\Delta E_y(0)L\right]\simeq\left(2/L^2\right)V_{DS} \tag{4-36}$$

as the incremental longitudinal field at the source is much less than average field $V_{DS}/L$. Following the mathematical derivation in [67], and inserting the condition that $\Delta\psi_{sb}$ equals zero, when the back surface is accumulated and $\Delta Q_{cb}$ equals zero, when the back surface is depleted, a general expression for $\Delta Q_{cf}(y)$ as a function of $\Delta\psi_{sf}(y)$ can be obtained as:

$$\Delta Q_{cf}(y)=C_{of}(1+\alpha)\Delta\psi_{sf}(y)-\beta\varepsilon_s t_b\eta/2 \tag{4-37}$$

where $\alpha = C_b/C_{of}$ and $\beta = 1$ for accumulation at the back surface, and for depletion at the back surface $\alpha = C_bC_{ob}/((C_b + C_{ob})\,C_{of})$ and $\beta = 1 + C_b/(C_b + C_{ob})$.

To get the general expression for $V_{DS} > 0$, the incremental surface potentials and charges are added to the solution for $V_{DS} = 0$.

The steady-state channel current in the triode mode of operation is:

$$I_{DS}=-WQ_{cf}(y)v(y) \tag{4-38}$$

Using a piecewise-continuous model for the carrier velocity in the channel [66]:

$$v(y) = \frac{\mu_{eff} |E(y)|}{1 + \mu_{eff} |E(y)| / 2v_{SAT}}, \quad for\, v(y) \le v_{SAT}$$
$$= v_{SAT}, \qquad otherwise \tag{4-39}$$

where $\mu_{eff}$ is the low-(longitudinal)-field mobility, which is affected by the transverse field $E_x$ in the channel. The dependence along the channel is modeled in terms of average field, $\overline{E_x}(y)$ in the channel [67]:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta \overline{E_x}(y)} \tag{4-40}$$

The average transverse field in the channel, from the solution of $V_{DS} = 0$ and $V_{DS} > 0$ is expressed as [67]:

$$\overline{E_x}(y) = \frac{C_{of}}{2\varepsilon_s}\left[V_{GfS} - V_{Tf} - \frac{Q_{b(eff)}}{C_{of}} + 2\frac{C_b}{C_{of}}(\psi_1 - \psi_{sb0}) + \beta\frac{C_b}{C_{of}}\left[\frac{t_b}{L}\right]^2 V_{DS} - (1-\alpha)\Delta\psi_{sf}(y)\right] \tag{4-41}$$

where $\alpha$ and $\beta$ are as defined previously. With (4-41), (4-40) can be rewritten as:

$$\mu_{eff} = \frac{\mu}{1 - B\Delta\psi_{sf}(y)} \tag{4-42}$$

where $\mu$ and $B$ are bias-dependent but spatially constant parameters [67]. Using the velocity expression given by (4-39) and the effective mobility expression given by (4-42), (4-38) can be written as:

$$-I_{DS}\left(1 - B\Delta\psi_{sf}\right) = \frac{I_{DS}\mu}{2v_{SAT}}\frac{d\psi_{sf}}{dy} + WQ_{cf}\mu\frac{d\psi_{sf}}{dy} \tag{4-43}$$

Integrating (4-43) from the source ($y = 0$) to drain ($y = L$), we get the drain current in the linear region as:

$$I_{DS} = \frac{W\mu_{eff}\left(Q_{cf}^2(0) - Q_{cf}^2(L)\right)}{2C_{of}(1+\alpha)L\left(1 + \left(\mu_{eff}/2v_{SAT}L\right)V_{DS}\right)} \tag{4-44}$$

where $\overline{\mu_{eff}} = \frac{\mu}{1 - f_B B V_{DS}}$ and $f_B$ is defined such that $\int_0^L \Delta\psi_{sf} dy \equiv f_B V_{DS} L$. In the saturation mode of operation, a high longitudinal electric field occurs near the drain, causing the carrier velocity to saturate. The channel current in saturation mode can be expressed as:

$$I_{DS} = -WQ_{cf}(L_e) v_{SAT} \tag{4-45}$$

where $L_e < L$ due to channel length modulation. In the saturation mode, the channel is divided into two regions, one in which the velocity is field dependent and the other in which the velocity is saturated. At the boundary between two regions, $y = L_e$, $V_{DS(eff)}$ equals $\Delta\psi_{sf}(L_e)$. In the region $0 \le y \le L_e$, (4-44) with $L$ and $V_{DS}$ replaced by $L_e$ and $V_{DS(eff)}$ expresses $I_{DSAT}$, which when equated to (4-45) gives $V_{DS(eff)}$ as a function of $L_e$. To fully characterize $I_{DSAT}$, another expression relating $V_{DS(eff)}$ and $L_e$ is needed to get the solution for $L_e$.

A cross section of SOI MOSFET is shown in Fig. 4.5. Gauss's law is applied to

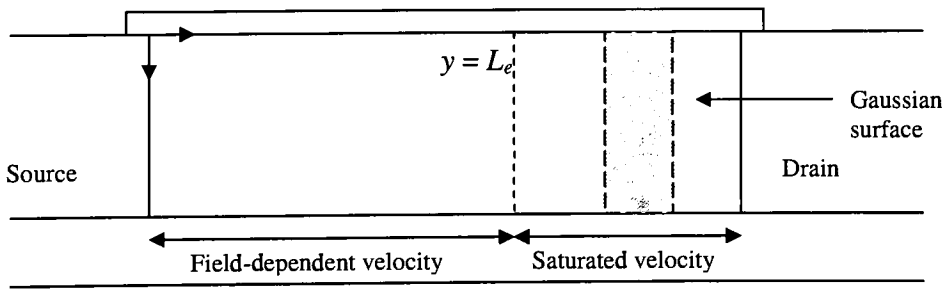


Fig. 4.5: Schematic cross section along the length of the channel, with SOI MOSFET in saturation showing field dependent and saturated velocity regions.

the shaded narrow strip shown in the region to derive a differential equation in $\Delta\psi_{sf}(y)$ [67]:

$$\varepsilon_s \frac{d^2}{dy^2}\left[\int_0^{t_b} \Delta\psi dx\right] = C_{of}\Delta\psi_{sf} + C_{ob}\Delta\psi_{sb} - \Delta Q_{cf} - \Delta Q_{cb} \tag{4-46}$$

Using $\Delta\psi_{sf}(L_e) = V_{DSeff}$ and with $\alpha$, $\beta$ and $\eta$ previously defined, following [67], a second-order differential equation can be obtained as:

$$\frac{d^2}{dy^2}\left(\Delta\psi_{sf}\right) = \frac{2C_{of}\left(1+\alpha\right)\left(\Delta\psi_{sf} - V_{D(SAT)}\right)}{C_b t_b^2 \beta} + \frac{2\eta}{\beta} \tag{4-47}$$

The boundary conditions for (4-47) are:

$\frac{d\left(\Delta\psi_{sf}\right)}{dy} = \frac{2v_{SAT}}{\mu_{eff}}$ at $y = L_e$ and $\Delta\psi_{sf}\left(L\right) = V_{DS}$. The solution of (4-47), for $t_b < L$, gives [67]:

$$L - L_e = L_d \approx l_c \sinh^{-1}\left[\frac{\overline{\mu_{eff}}\left(V_{DS} - V_{DS(eff)}\right)}{2v_{SAT} l_c}\right] \tag{4-48}$$

where,

$l_c = t_b\left[\frac{C_b\beta}{2C_{of}\left(1+\alpha\right)}\right]^{1/2}$ and,

$L_d$ is length of high field region. The combination of the expression for $V_{DS(eff)}$ discussed previously and (4-48) gives a transcendental equation for $L_e$ that can be solved numerically in few iterations. Once the value of $L_e$ is found out, the drain current in saturation region can be calculated. A block diagram describing steps for numerical simulation of $I - V$ characteristics in SOI MOSFETs is shown in Fig. 4.6. A single-gate SOI MOSFET and a double-gate SOI MOSFET were simulated and verified with experimental data using the above described model.

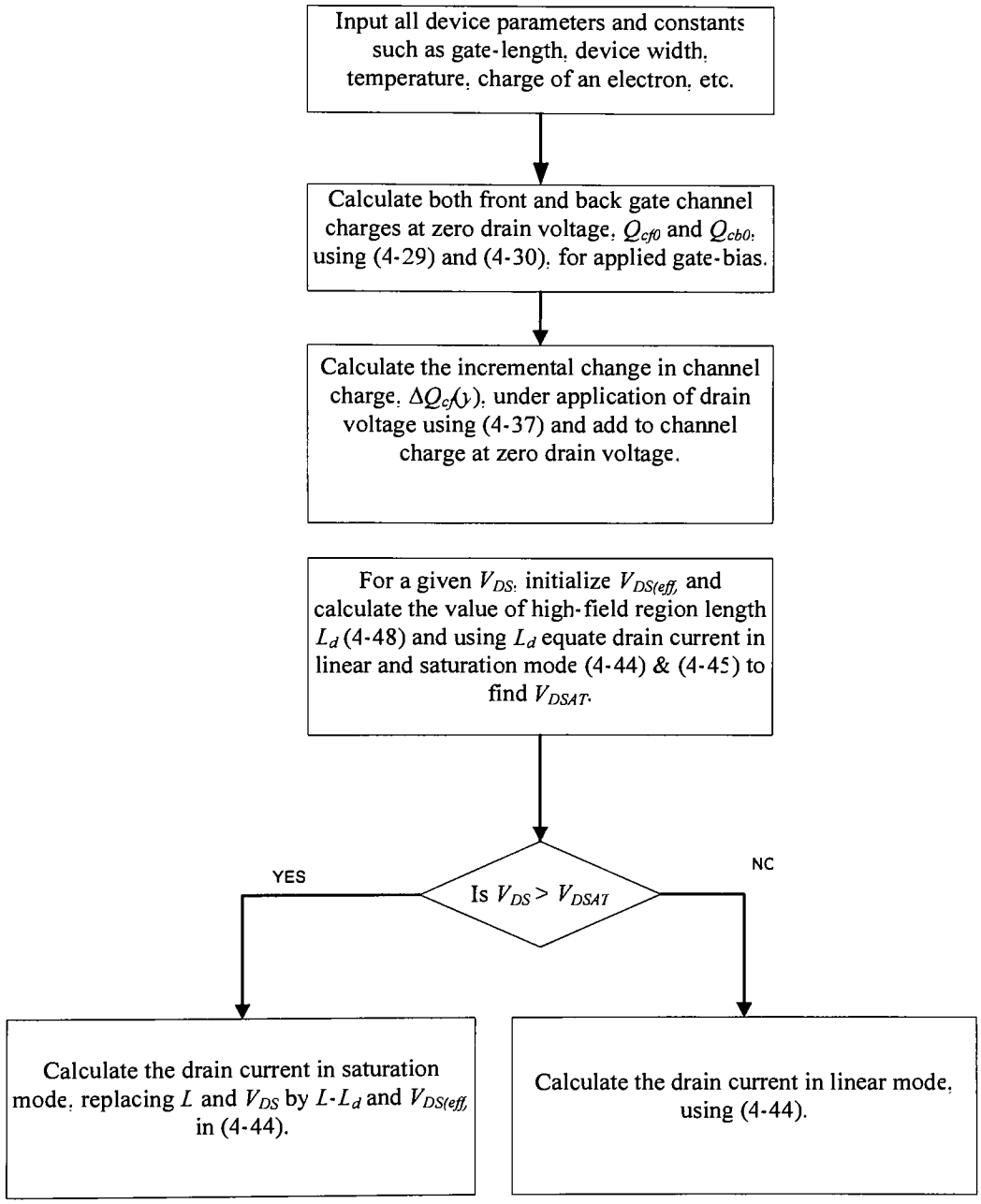


Fig. 4.6: Block diagram to model $I - V$ characteristic in SOI MOSFETs.

*Chapter 5*

# Results and analysis



## 5.1 Quantum modeling results

With the quantum mechanical model, as explained in **Chapter 3** (Section. 3.3), the inversion charge has been calculated in a single-gate (BULK) MOSFET, a single-gate (SOI) MOSFET and a double-gate (SOI) MOSFET. The quantum mechanical model was developed and simulated by Islam[1].

The variation in inversion charge density ($N_{inv}$) with respect to applied gate voltage for a submicron ($L_G$ = 0.25 μm) single-gate (bulk) NMOS device for different silicon doping levels is shown in Fig. 5.1. As explained in **Chapter 4** (Section 4.2), the threshold voltage for the device is defined as the voltage where gate-to-channel capacitance reaches one-third of its maximum value. The peak of the derivative of channel capacitance with respect to applied gate-to-source voltage coincides with the $V_{GS}$ at which the gate-to-channel capacitance has risen to one-third of its maximum value and that voltage is defined as threshold voltage. For a single-gate (bulk) n-channel FET, the threshold voltage changes from 0.11 V to 0.65 V as the p-type substrate doping

[1]Dr Syed S. Islam, Private Communication

concentration changes from $1 \times 10^{17}$ $cm^{-3}$ to $8 \times 10^{17}$ $cm^{-3}$. For the 0.25 μm single-gate (Bulk) MOSFET ($N_A = 4 \times 10^{17}$ $cm^{-3}$, $t_{ox} = 5.6$ nm), 0.91 μm single-gate (SOI) MOSFET (($t_{ox} = 10$ nm, $t_{Si} = 95$ nm, $N_A = 1 \times 10^{15}$ $cm^{-3}$) and 0.33 μm double-gate ($t_{ox} = 11$ nm, $t_{Si} = 60$ nm, $N_A = 1 \times 10^{15}$ $cm^{-3}$) NMOS under consideration, it was found to be 0.46 V, -0.1 V and –0.13 V, respectively.

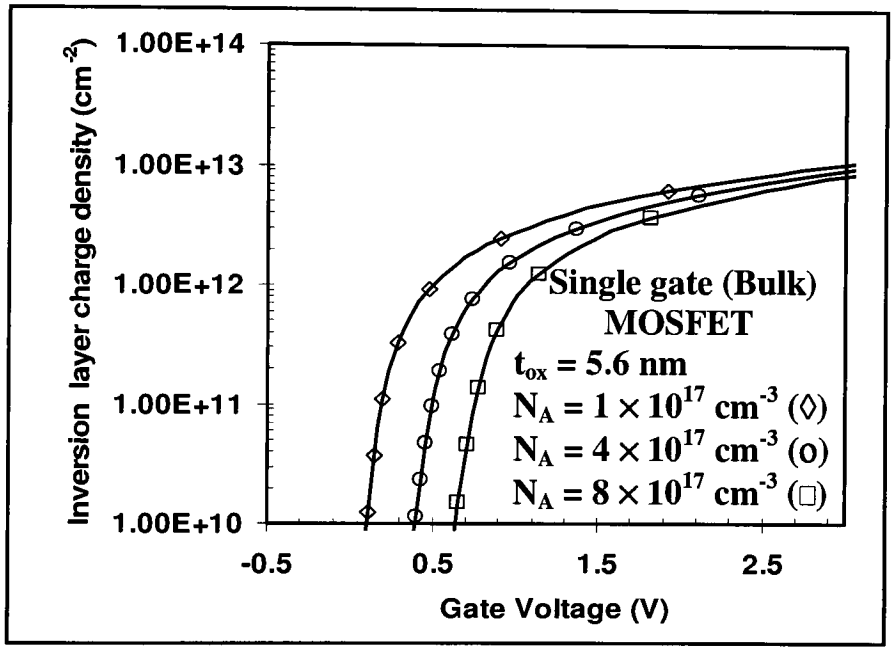


Fig. 5.1: Inversion charge density for single-gate (Bulk) MOSFET ($N_A = 1 \times 10^{17}$ $cm^{-3}$ (◊), $4 \times 10^{17}$ $cm^{-3}$ (o) and $8 \times 10^{17}$ $cm^{-3}$ (□)).

The variation in inversion charge density with respect to applied gate voltage for a 0.91 μm single-gate (SOI) NMOS device for silicon doping of $1 \times 10^{15}$ $cm^{-3}$ is shown in Fig. 5.2. Fig. 5.3 shows the variation in inversion charge density with respect to applied gate voltage for a 0.33 μm double-gate (SOI) NMOS device with p-type substrate and silicon doping concentration of $1 \times 10^{15}$ $cm^{-3}$ and oxide thickness 11 nm.

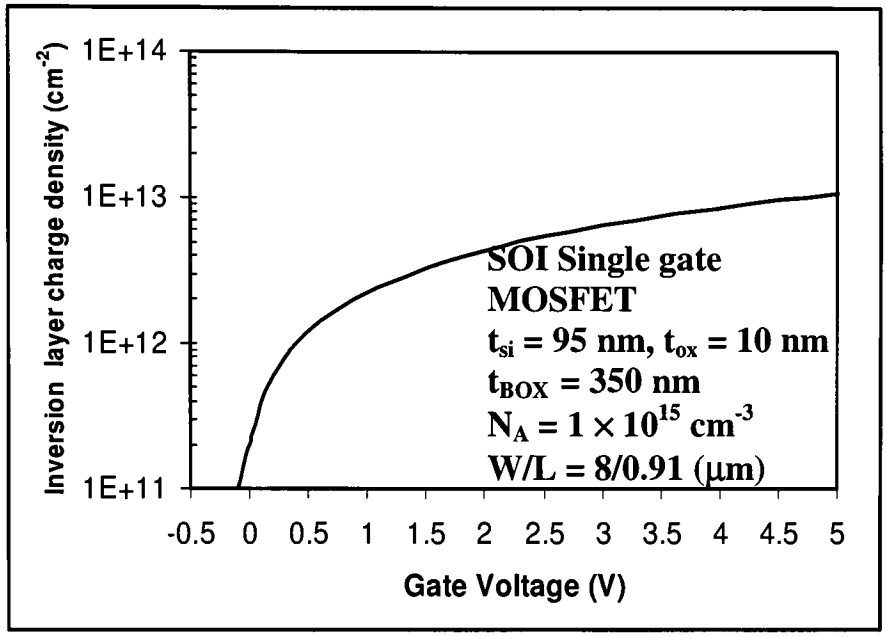


Fig. 5.2: Inversion charge density for single-gate (SOI) MOSFET ($N_A$ = 1× $10^{15}$ $cm^{-3}$).

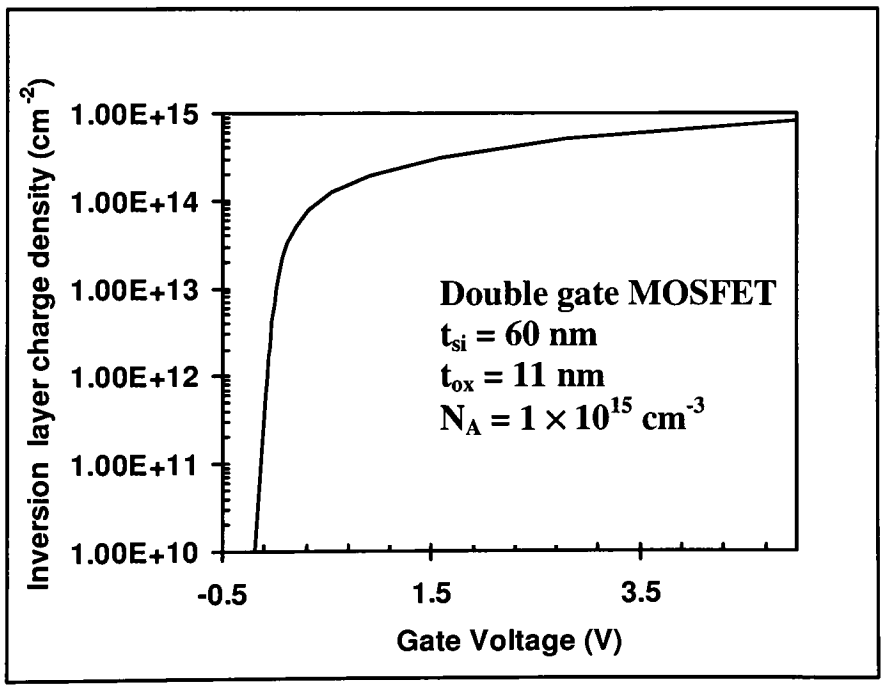


Fig. 5.3: Inversion charge density for double-gate (SOI) MOSFET ($N_A$ = 1× $10^{15}$ $cm^{-3}$).

As expected, the inversion charge density is greater in the double-gate device because of the effects of two symmetrical gates. The distribution of inversion charge density with respect to channel depth for various silicon thicknesses for a double-gate MOSFET is shown in Fig. 5.4. The threshold voltage changes from –0.012 V to –0.007 V as silicon thickness ($t_{Si}$) changes from 5 nm to 7 nm. As seen, the inversion charge concentration is higher in double-gate with lower silicon thickness.

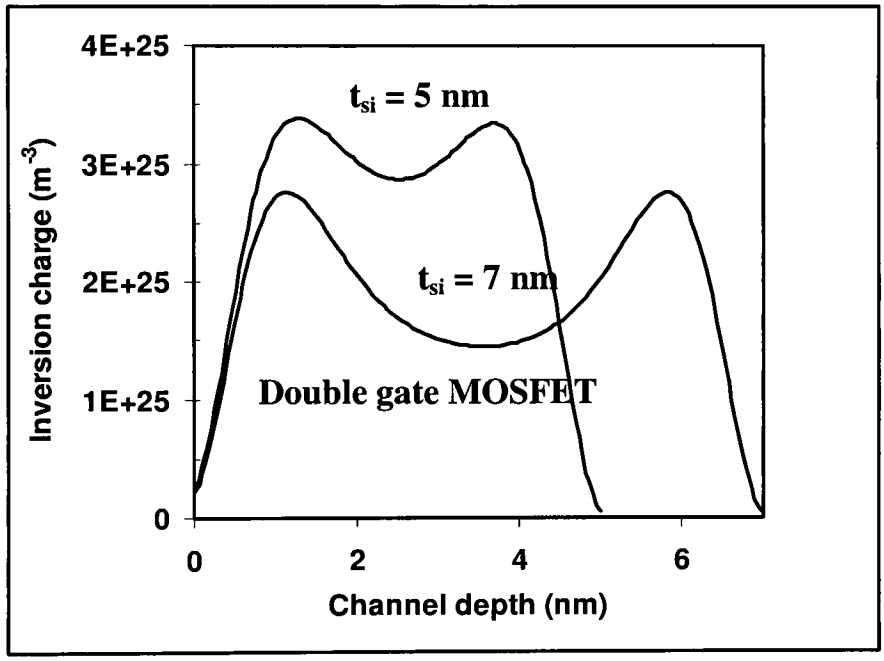


Fig. 5.4: Inversion charge profile of double-gate MOSFET for different silicon thicknesses ($t_{Si}$ = 5 nm, $t_{Si}$ = 7 nm, $N_A = 1\times 10^{15}$ cm$^{-3}$)

Fig. 5.5 and Fig. 5.6 show variation of gate-to-channel capacitance ($C_{gc}$) with applied gate voltage for single-gate (Bulk) and single-gate (SOI) MOSFET, respectively.

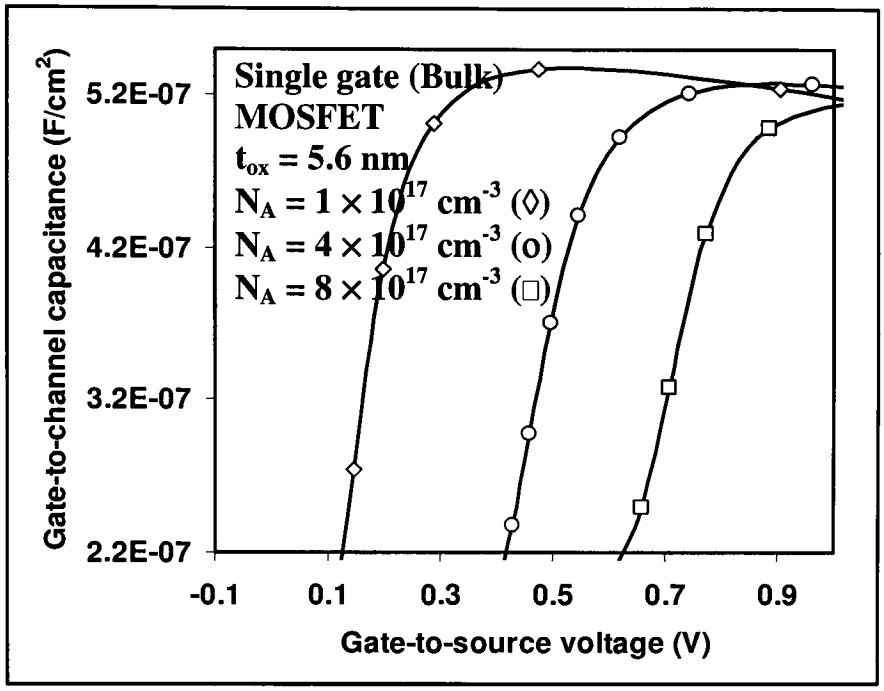


Fig. 5.5: Plot of channel-to-gate capacitance for single-gate (Bulk) MOSFET ($N_A = 1\times 10^{17}$ cm$^{-3}$ (◊), $4 \times 10^{17}$ cm$^{-3}$ (o) and $8 \times 10^{17}$ cm$^{-3}$ (□)).

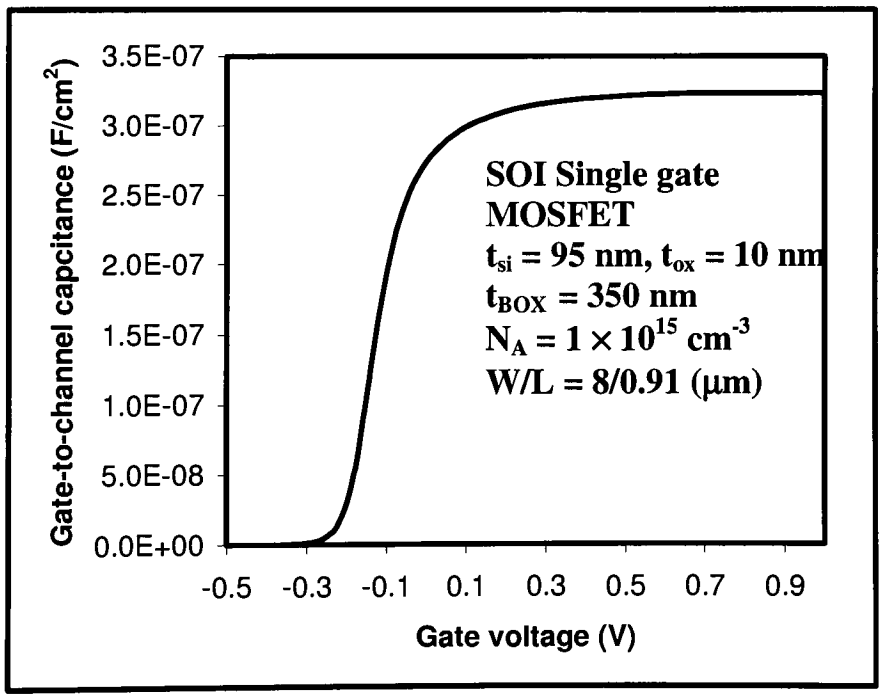


Fig. 5.6: Plot of channel-to-gate capacitance for single-gate (SOI) MOSFET ($N_A = 1\times 10^{15}$ cm$^{-3}$).

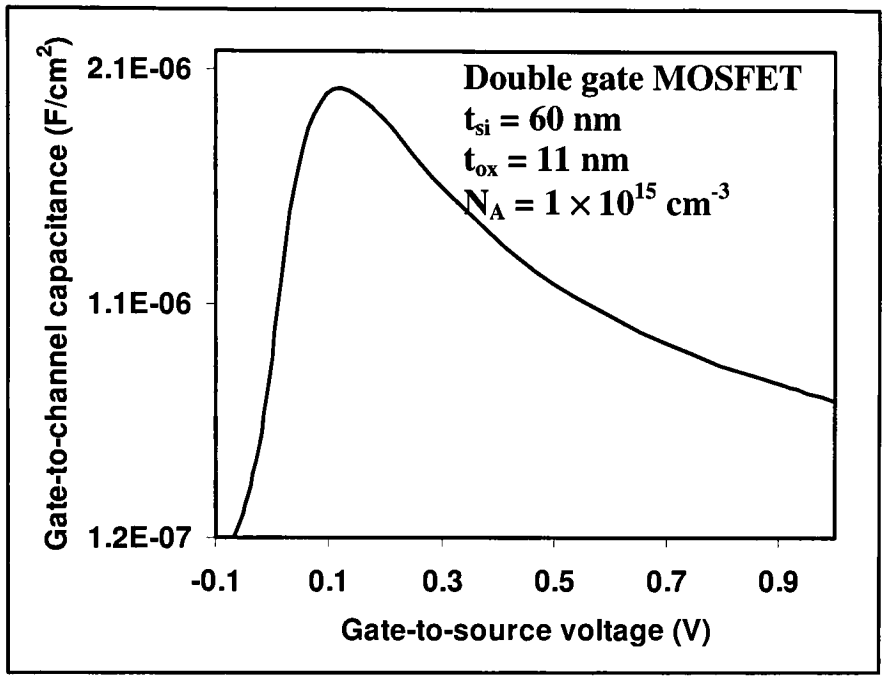


Fig. 5.7: Plot of channel-to-gate capacitance for double-gate (SOI) MOSFET ($N_A = 1\times 10^{15}$ cm$^{-3}$).

Fig. 5.7 shows variation of gate-to-channel capacitance ($C_{gc}$) with applied gate voltage for double-gate (SOI) MOSFET. Again, as expected $C_{gc}$ is higher for double-gate than single-gate. The roll-off observed for gate-to-channel capacitance in double-gate device in Fig. 5.7 for $V_{GS} > 0.1$ V can be attributed to small silicon film thickness and polysilicon gate depletion. In modern MOSFET technologies, polysilicon is heavily doped to have conducting characteristics like a metal [32]. At higher applied gate-bias, the depletion region is formed under the gate resulting in thickening of the effective oxide thickness. The resulting small value of the capacitance becomes a dominant factor at higher gate bias as it is in series with gate capacitance component associated with the oxide layer.

## 5.2 *I-V* modeling results

The *I-V* model developed in **Chapter 4** (Section. 4.3) is used to simulate a single-gate (Bulk) MOSFET and the results have been matched with experimental data [68]. Table. 5.1 lists the parameters used for simulation.

Table 5.1: Single-gate (Bulk) n-channel MOSFET parameters.

| Device parameters | Value |
|---|---|
| Substrate doping, $N_{sub}$ ($cm^{-3}$) | $4\times10^{17}$ |
| Oxide thickness, $t_{ox}$ (nm) | 5.6 |
| Width (μm) | 10 |
| Length (μm) | 0.25 |
| Junction depth, $x_j$, (μm) | 0.16 |
| Low-field mobility ($cm^2$/V-sec) | 600 |
| Oxide field effect parameter, $\theta$, ($V^{-1}$) | 0.055 |
| Saturation velocity, $V_{SAT}$, (cm/sec) | $1 \times 10^7$ |

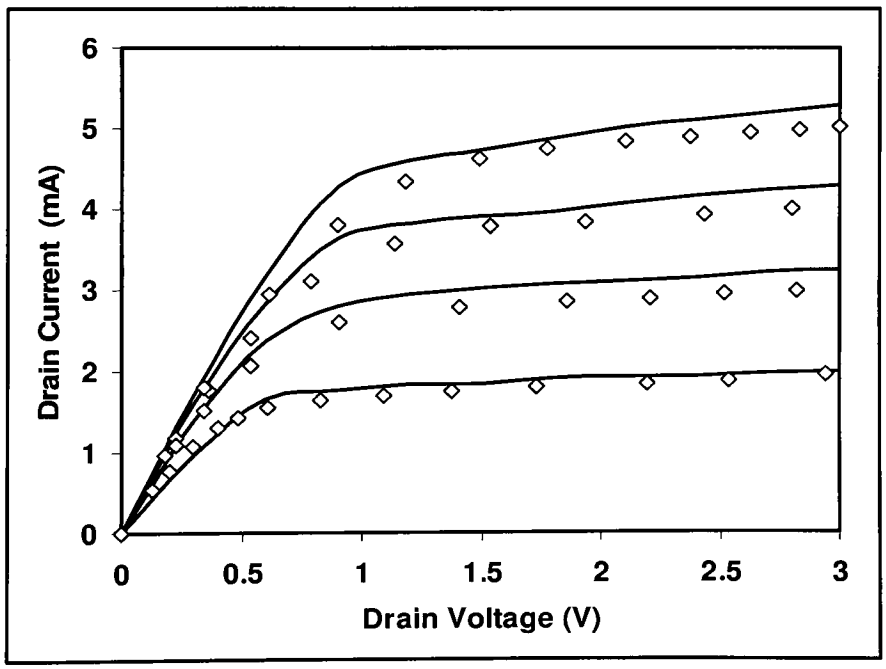


Fig. 5.8: Comparison of calculated *I-V* characteristics of single-gate (Bulk) MOSFET (solid line) with measurement [68] (symbols). Top curve: $V_{GS}$ = 3.0 V, step: -0.5 V

The only adjusting parameter used in the model is the field, $E_c$ which has been used as a varying parameter to calculate the lateral field at the transition point. The value of $E_c$ used in this work is 0.6 $\times 10^4$ V/cm. Fig. 5.8 shows the calculated $I_{DS}$-$V_{DS}$ characteristics and a comparison with experimental data for single-gate (Bulk) [68] MOSFET.

The parameters used for the simulation of single- and double-gate (SOI) MOSFET are listed in Table. 5.2 and Table 5.3, respectively. Fig. 5.9 and Fig. 5.10 show the calculated $I_{DS}$-$V_{DS}$ characteristics using the *I-V* model developed in **Chapter 4** (Section. 4.4) and a comparison with experimental data for a single- [69] and a double-gate (SOI) [70] MOSFET, respectively.

Table. 5.2: Single-gate (SOI) n-channel MOSFET parameters.

| Device parameters | Value |
|---|---|
| Substrate doping, $N_{sub}$ ($cm^{-3}$) | $1\times10^{15}$ |
| Silicon film thickness, $t_{si}$ (nm) | 95 |
| Oxide thickness, $t_{ox}$ (nm) | 10 |
| Buried oxide thickness, $t_{BOX}$ (nm) | 350 |
| Width (μm) | 8 |
| Length (μm) | 0.91 |
| Low-field mobility ($cm^2$/V-sec) | 1000 |
| Saturation velocity, $V_{SAT}$, (cm/sec) | $1\times10^{7}$ |

Table. 5.3: Double-gate (SOI) n-channel MOSFET parameters.

| Device parameters | Value |
|---|---|
| Substrate doping, $N_{sub}$ ($cm^{-3}$) | $1\times10^{15}$ |
| Silicon film thickness, $t_{si}$ (nm) | 60 |
| Oxide thickness, $t_{ox}$ (nm) | 11 |
| Width (μm) | 10 |
| Length (μm) | 0.33 |
| Low-field mobility ($cm^2$/V-sec) | 900 |
| Saturation velocity, $V_{SAT}$, (cm/sec) | $1\times10^{7}$ |

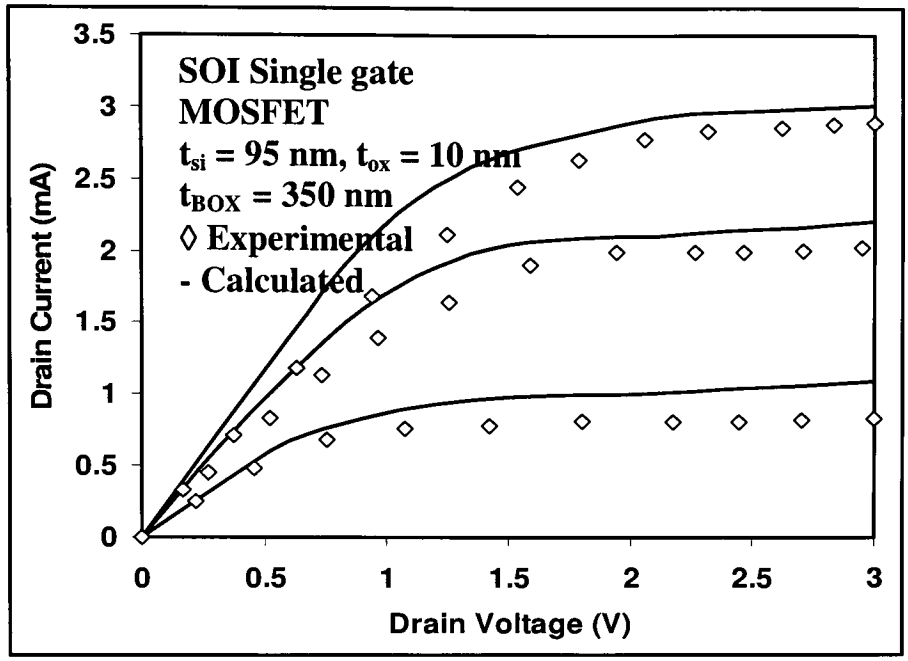


Fig. 5.9. Comparison of calculated *I-V* characteristics of single-gate (SOI) MOSFET (solid line) with measurement [69] (symbols). Top curve: $V_{GS}$ = 3.0 V, step: -1.0 V

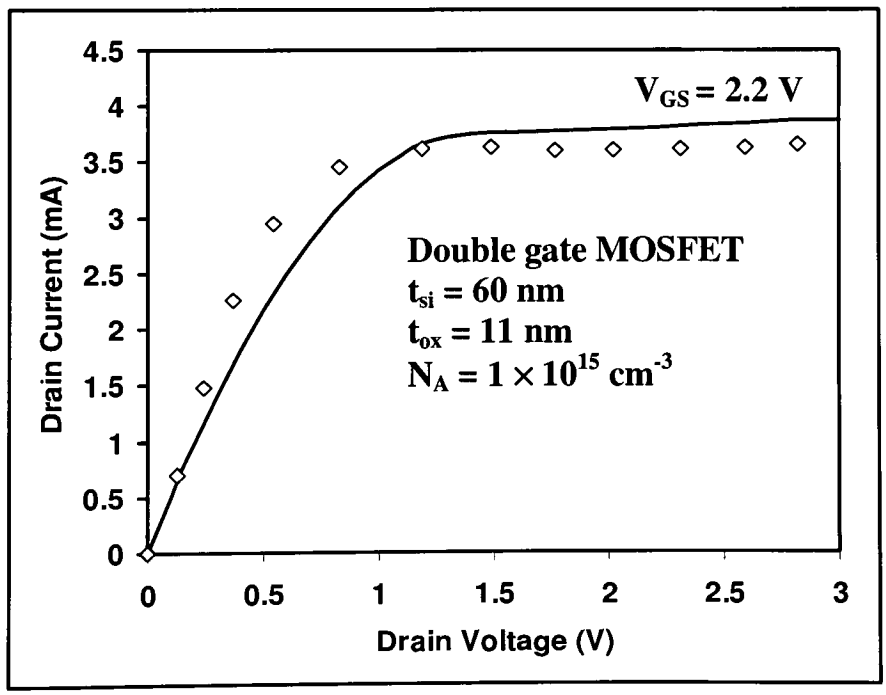


Fig. 5.10. Comparison of calculated *I-V* characteristics of double-gate (SOI) MOSFET (solid line) with measurement [70] (symbols).

The discrepancy observed in the simulated results as compared with the experimental data of drain current for the MOSFETs under study can be explained on the basis of channel carrier transport model used in characterizing the drain current, the effect of source-drain parasitic resistances, the effect of increase in effective thickness gate oxide due to shape of the inversion region, polysilicon gate depletion, electron tunneling through gate insulator due to thin gate oxide *etc* [32]. The $I - V$ models used in this work does not account for the effect of gate capacitance component associated with gate depletion and electron tunneling through gate. The two-piece carrier velocity model used in this work does not predict the *parabolic* dependence of carrier velocity on lateral electric field accurately, as observed in the literature [71] and overestimates the drain current in the device. The parabolic dependence of electron drift velocity is modeled using an empirical expression in [72], and can be used to get better match of $I - V$ characteristics. The source-drain resistance reduces the value of the MOSFET drain current and accurate prediction of source-drain resistance is very important for calculating the drain current.

### 5.3 Low frequency noise modeling results

After modeling the inversion charge in the devices and calculating the drain current, the low frequency noise model developed in **Chapter 2** (Section. 2.3) is used to calculate the bias dependence of low-frequency drain current noise spectrum ($A^2$/Hz) for the devices under consideration. The drain current noise spectrum has been calculated for varying drain voltage at fixed gate bias and also for varying gate bias at fixed drain voltage. All the calculations are done at frequency, $f$ = 100 Hz and at temperature, $T$ =

300 K. At such a low frequency, thermal noise in MOSFETs is negligible as compared to flicker noise. As mentioned earlier (Section 2.2.2), Hooge's parameter should be modified for MOSFETs as more than one scattering mechanism exist. Although in this work, the Hooge's parameter has been taken as constant, it is found to be dependent on applied gate bias and oxide thickness [46]. The measured value of Hooge's parameter for MOSFETs is consistently smaller than $2 \times 10^{-3}$, the value predicted by Hooge for homogeneous samples. The value of Hooge's parameter used in this work for the n-channel bulk MOSFTET and the n-channel SOI MOSFET is $2.9 \times 10^{-6}$ [71] and $7 \times 10^{-4}$ [72]. The low frequency drain current noise power with respect to applied gate bias based on the flicker noise model developed in this work for a single-gate (Bulk) n-channel MOSFET fabricated by a conventional 3 μm CMOS technology ($N_A = 1 \times 10^{15}$ cm$^{-3}$, $t_{ox} = 50$ nm, $W = 9.5$ μm, $L = 4.5$ μm) is shown and compared with experimental data [25] in Fig. 5.11.

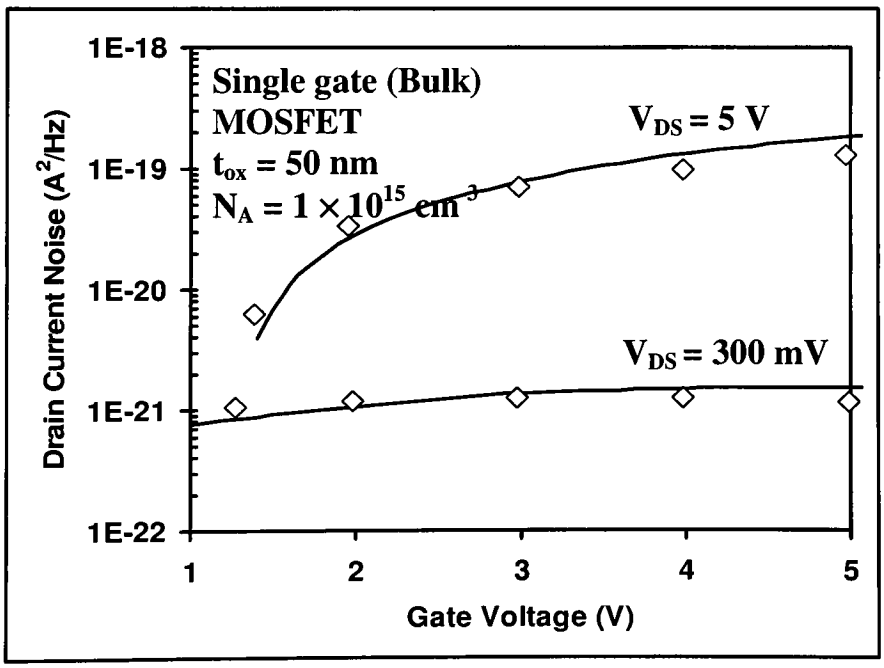


Fig. 5.11: Comparison of calculated (solid line) drain current noise power of single-gate (Bulk) MOSFET, $L = 4.5$ μm with varying gate bias at frequency, $f = 100$ Hz with measurements (symbol) [25].

The solid line represents simulation results based on the noise model, whereas the symbols are measurements. An excellent agreement between measurement and simulation is observed. The drain current noise power is observed to change as the device region of operation changes from weak inversion to strong inversion, with varying gate voltage. The low frequency drain current noise power with respect to applied gate bias based on the flicker noise model developed in this work for a submicron single-gate (Bulk) n-channel MOSFET, $L$ = 0.25 μm is shown in Fig. 5.12. Fig. 5.13 shows the low frequency drain current noise power with respect to applied drain bias at fixed gate voltage for the submicron single-gate (Bulk) n-channel MOSFET. The drain current noise power has been calculated in strong inversion and it tends to saturate once the drain current ceases to increase with the drain voltage.

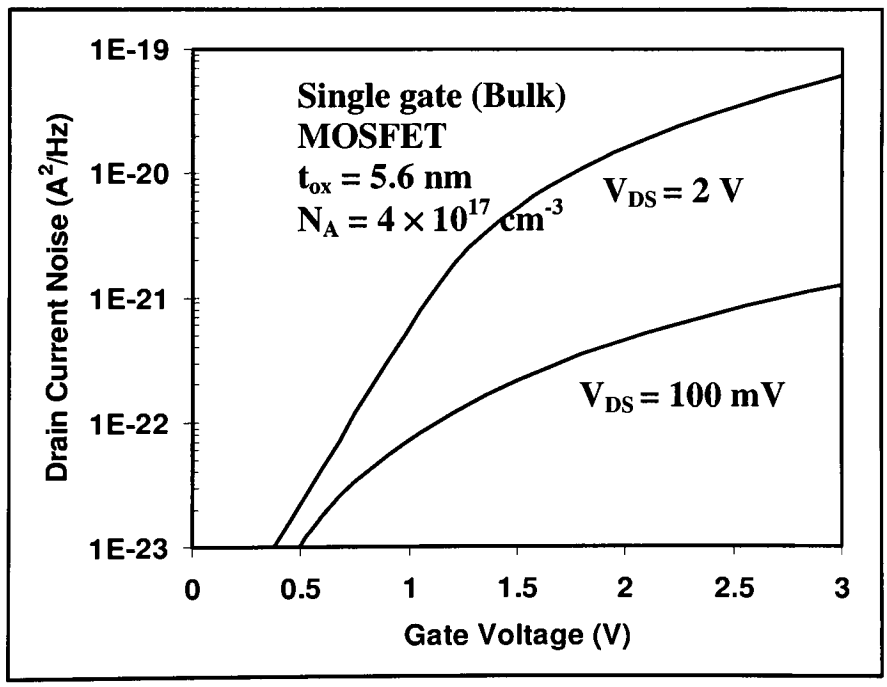


Fig. 5.12: Calculated drain current noise power of single-gate (Bulk) MOSFET, $L$ = 0.25 μm with varying drain bias at frequency, $f$ = 100 Hz.

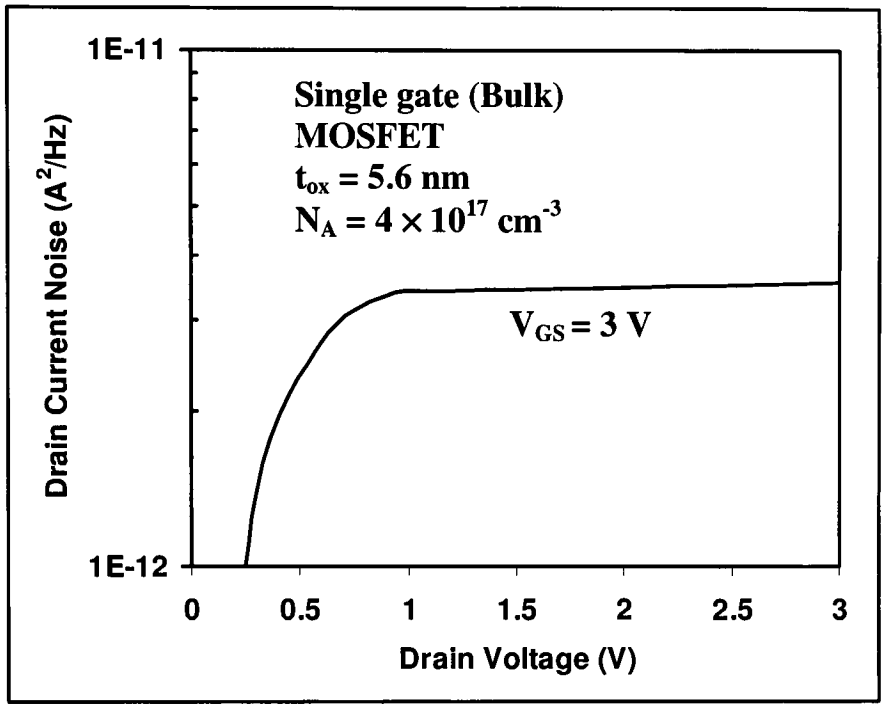


Fig. 5.13: Calculated drain current noise power of single-gate (Bulk) MOSFET, $L = 0.25$ μm with varying drain bias at frequency, $f = 100$ Hz.

The low frequency drain current noise power with respect to applied gate bias based on the flicker noise model for the considered single-gate (SOI) n-channel MOSFET is shown in Fig. 5.14. Fig. 5.15 shows the low frequency drain current noise power with respect to applied drain bias at fixed gate voltage for the considered single-gate (SOI) n-channel MOSFET.

The difference in drain current noise power of a single-gate (SOI) n-channel MOSFET compared to that of a single-gate (Bulk) n-channel MOSFET can be attributed to differences in inversion charge carrier density, oxide trap energy density, effective mobility fluctuations and Hooge's parameter.

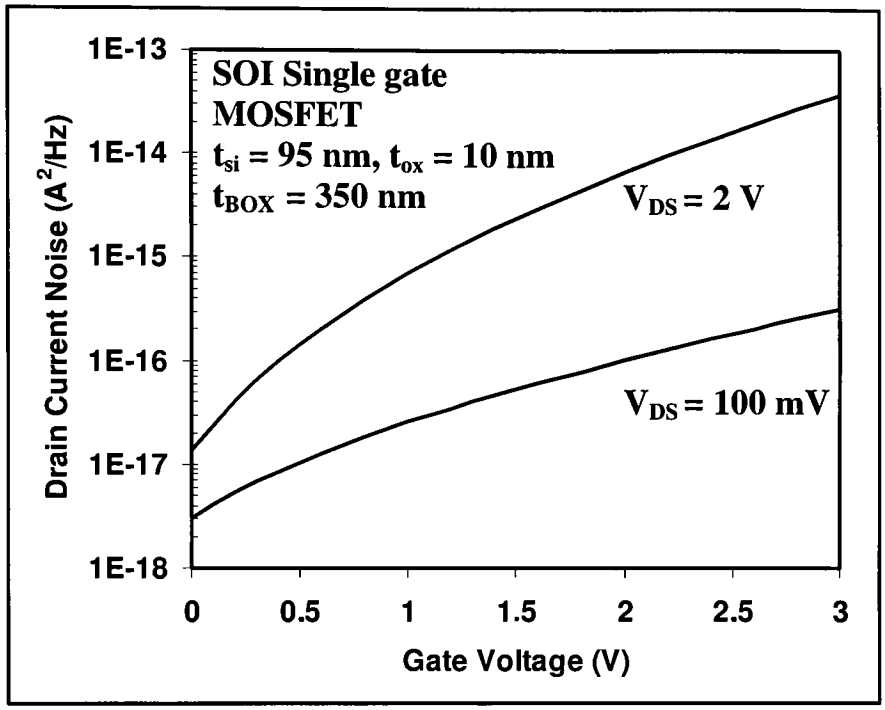


Fig. 5.14: Calculated drain current noise power of single-gate (SOI) MOSFET with varying gate bias at frequency, $f$ = 100 Hz.

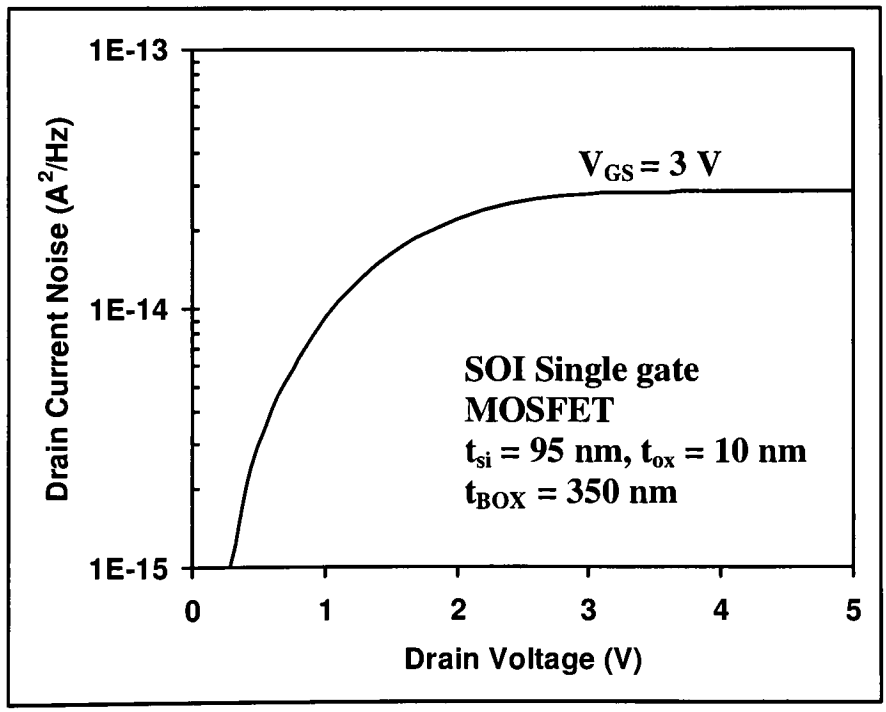


Fig. 5.15: Calculated drain current noise power of single-gate (SOI) MOSFET with varying drain bias at frequency, $f$ = 100 Hz.

The calculated drain current noise power for the considered double-gate (SOI) MOSFET for varying gate bias is shown in Fig. 5.16. As expected, the drain current noise power in the double-gate device is comparatively higher than in the single-gate device owing to the fact that inversion charge carrier density in the double-gate device is greater than in the single-gate device. Fig. 5.17 shows the drain bias dependence of the drain current noise power of the considered double-gate (SOI) device, for a fixed gate bias.

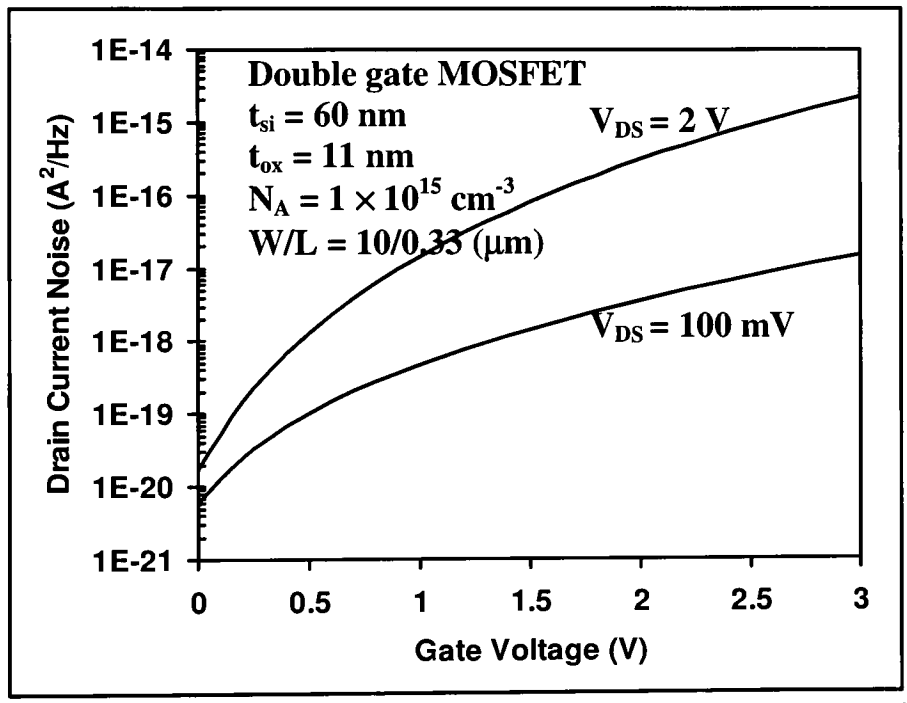


Fig. 5.16: Calculated drain current noise power of double-gate (SOI) MOSFET with varying gate bias at frequency, $f$ = 100 Hz.

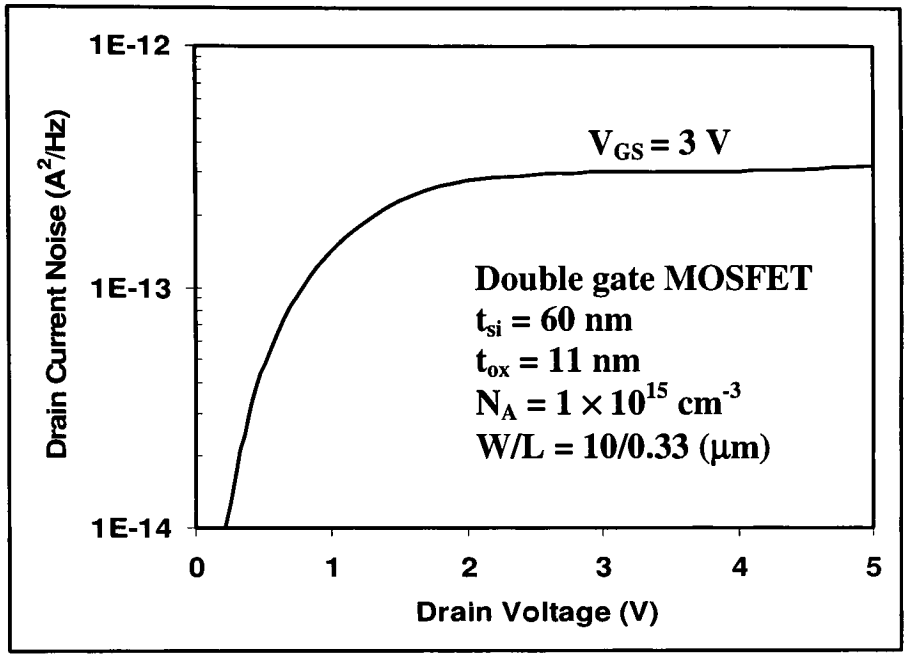


Fig. 5.17: Calculated drain current noise power of double-gate (SOI) MOSFET with varying drain bias at frequency, $f$ = 100 Hz.

Also, higher drain current noise power in SOI devices than in bulk devices can be explained by the higher value of Hooge's parameter in SOI devices than in bulk devices, as the drain current noise power is directly proportional to Hooge's parameter in the low frequency noise model.

*Chapter 6*

# Conclusions and Future Work



## 6.1 Conclusions

The low frequency noise ($1/f$) of MOSFETs plays critical roles in determining characteristics of analog and RF circuits such as oscillator phase noise, and dynamic range of broadband amplifiers. Therefore its origin, related $1/f$ noise theories, and its modeling have been studied.

In **Chapter 2**, in order to study and analyze $1/f$ noise of MOSFETs, the fundamental features of a MIS (Metal-Insulator-Semiconductor) system such as traps, and barrier heights, as well as physical nature of electrons and holes are discussed because these are directly involved in the $1/f$ noise generation mechanisms such as trapping-detrapping. Also, several existing $1/f$ noise models such as the number fluctuation model, the mobility fluctuation model, and the correlated model have been discussed to better understand the noise generation mechanism. An extension of the correlated model is developed and described.

**Chapter 3** discusses the inversion charge density modeling in MOSFETs. The limitations of the classical model to accurately predict inversion charge density and the

need for quantum mechanical modeling have been discussed. The quantum mechanical model based on self-consistent solution of Poisson- Schrödinger equations and Fermi-Dirac statistics has been explained. The quantum calculations have been used to accurately predict the threshold voltage of devices.

In **Chapter 4**, the types of devices under consideration and their $I - V$ modeling is described. Modeling of single-gate bulk MOSFET and single- and double-gate SOI MOSFET is discussed in detail. The calculation of threshold voltage using a unified charge control model has been explained.

Finally in **Chapter 5**, results of quantum mechanical modeling, $I - V$ modeling of devices under study, and low frequency noise modeling have been presented.

In summary, the fundamentals of $1/f$ noise, the $1/f$ noise generation mechanisms, and modeling of $1/f$ noise have been studied in this work. The model developed takes into account the quantization of energy levels in the potential well formed at semiconductor-insulator interface in MOSFETs, short-channel effects in $I - V$ modeling of devices, and correlated $1/f$ noise generation mechanisms.

## 6.2 Future work

The model developed in this work has used Hooge's parameter as an empirical constant. The dependence of Hooge's parameter on applied gate bias and oxide thickness can be studied and incorporated in the low frequency noise model. The $I - V$ modeling in this work can be used to develop a small-signal model of devices under study, and

subsequently a high frequency model can be developed to explain the complete noise behavior of devices.

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# Appendix



**Derivation of (2-12)**

The coordinates $x$, $y$, and $z$ correspond to the coordinates as shown in Fig. 2.1. According to number fluctuation theory, the power spectral density of the mean square fluctuation in the number of occupied traps is given as:

$$S_{\Delta N_t}(y,f) = \int_{E_v}^{E_c} \int_0^{W} \int_0^{T_{ox}} 4N_t(E,x,y,z)\Delta y f_t(1-f_t)\cdot\frac{\tau(E,x,y,z)}{1+\omega^2\tau^2(E,x,y,z)}\Delta z\Delta x\Delta E \qquad \text{(A-1)}$$

where,

$f_t = [1+\exp(E_t - E_{fn})/kT]^{-1}$ is the trap occupancy function,

$E_{fn}$ is the electron quasi-Fermi level,

$\omega = 2\pi f$ is the angular frequency,

$N_t(E,x,y,z)$ is the distribution of the traps in the oxide and over the energy,

$\tau(E,x,y,z)$ is the trapping time constant, and

$T_{ox}$ is the oxide thickness, and $E_c - E_v$ is the silicon energy gap.

The trapping time constant is given by:

$$\tau = \tau_0(E)\exp(\gamma x) \qquad \text{(A-2)}$$

where, $\tau_0(E)$ is the time constant at the interface and $\gamma$ is the attenuation coefficient of the electron wave function in the oxide.

Choose $x_1$ such that the traps for $x > x_1$ have a time constant that is so long that their effect on the noise cannot be measured. Assuming a uniform trap distribution for $0 < x < x_1$ and zero traps outside, we get normalized distribution which can be expressed as:

$$\frac{\Delta x}{x_1} = \frac{\Delta\tau/\tau}{\ln(\tau_1/\tau_0)} = g(\tau)\Delta\tau \tag{A-3}$$

where $\tau_1$ is the time constant of trap at $x_1$. Replacing $\Delta x$ by $x_1 g(\tau)\Delta\tau$ and integrating (A-1) with respect to $\tau$ between the limits $\tau_0$ and $\tau_1$ we get:

$$S_{\Delta N_t}(y,f) = \int_{E_v}^{E_c}\int_0^W N_t(E,x,y,z)\Delta y f_t(1-f_t)\Delta z\Delta E\frac{x_1}{f\ln(\tau_1/\tau_0)} \tag{A-4}$$

for $1/\tau_1 < \omega < 1/\tau_0$. Since $f_t(1 - f_t)$ function has a sharp peak near quasi-Fermi level $E_{fn}$, introducing a parameter, $N_t(E_{fn})$ given as:

$$N_t(E_{fn}) = \int_{-\infty}^{\infty} N_t(E,x,y,z) f_t(1-f_t)\Delta E \tag{A-5}$$

and integrating (A-4) with respect to energy, we get:

$$S_{\Delta N_t}(y,f) = \int_0^W N_t(E_{fn})\Delta y\Delta z\frac{x_1}{f\ln(\tau_1/\tau_0)} \tag{A-6}$$

Next, integrating (A-6) with respect to $z$ between the limits 0 and $W$, we get, since $\ln(\tau_1/\tau_0) = \gamma x_1$ (from (A-2)) ,

$$S_{\Delta N_t}(y,f) = N_t(E_{fn})\Delta y\frac{Wx_1}{f\ln(\tau_1/\tau_0)} = \frac{N_t(E_{fn})\Delta y}{\gamma f} \tag{A-7}$$

**Derivation of (2-14)**

Following Section 2.3, the drain current noise power is given by (2-14):

$$S_{I_D}(f) = \frac{kTI_D^2}{\gamma f W L^2} \int_0^L N_t(E_{fn}) \left[ \frac{R}{N} + \alpha\mu_{eff} \right]^2 dy \tag{A-8}$$

The drain current, $I_D$ can be expressed as:

$$I_D = Wq(N)\mu_{eff} \frac{dV}{dy} \tag{A-9}$$

Also, rearranging the terms we can get:

$$N\left[ \frac{R}{N} + \alpha\mu_{eff} \right]^2 = \left(1 + \alpha\mu_{eff} NR^{-1}\right)^2 \frac{R^2}{N} \tag{A-10}$$

Using (A-9) and (A-10) in (A-8), and changing the limit of integration from 0 to $L$, to 0 to $V_D$, (A-8) can be expressed as:

$$S_{I_D}(f) = \frac{kTqI_D\mu_{eff}}{\gamma f L^2} \int_0^{V_D} N_t(E_{fn}) \left(1 + \alpha\mu_{eff} NR^{-1}\right)^2 \frac{R^2}{N} dV \tag{A-11}$$

**Derivation of (4-26)**

Following Section 4.3, the drain current in linear region is given as:

$$I_{DL} = W \mid Q_n(y) \mid v(y) \tag{A-12}$$

where,

$$Q_n(y) = C_{ox}\left[ V_G - V_T - 2a_0 V(y) \right] \tag{A-13}$$

Integrating over the channel length $L$ and following Section 4.3, the drain current is given by:

$$I_{DL} = W\mu_{eff}C_{ox}\frac{(V_{GS} - V_{TH} - a_0 V_{DS})V_{DS}}{L(1+V_{DS}/LE_c)} \quad \text{(A-14)}$$

In saturation region, substituting $V_{DS}$ with $V_{DSAT}$ in (A-13) and (A-14), and then equating (A-12) to the right hand side of (A-14), we get:

$$(V_{GS} - V_{TH} - 2a_0 V_{DSAT})E_{SAT} = \frac{(V_{GS} - V_{TH} - a_0 V_{DSAT})V_{DSAT}}{(L+V_{DS}/E_c)} \quad \text{(A-15)}$$

Rearranging the terms in (A-15), an expression between $V_{DSAT}$ and $E_{SAT}$ can be obtained as:

$$a_0 V_{DSAT}E_{SAT}(L+V_{DSAT}/E_c)+(V_G - V_T - a_0 V_{DSAT})\left(V_{DSAT} - LE_{SAT} - \frac{E_{SAT}V_{DSAT}}{E_C}\right) = 0 \quad \text{(A-16)}$$